

VIII THEORY OF OPERATION

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8.1 INTRODUCTION

This section concerns itself with the hardware aspects of the Sol Terminal Computer^{T.M.}. It specifically deals with the operation of the power supply and the logic associated with the Sol-PC and keyboard. Descriptions of software and the operation of the circuitry contained in the multitude of integrated circuits (IC's) used in the Sol fall outside the scope of this section. In some cases, references to other publications or sections in this manual are provided when it is felt that additional information will contribute to a better understanding of how Sol operates. Should the reader wish to delve further into the operation of a specific IC, we suggest that he study the appropriate data sheet for that IC.

The section begins with an overview of the Sol design. A block diagram analysis then provides the reader with an understanding of the relationship between the functional elements of the Sol-PC. This analysis sets the stage for detailed descriptions of the circuitry that makes up these elements. The section concludes with a block diagram analysis and circuit description of the keyboard.

8.2 OVERVIEW

The Sol Terminal Computer^{T.M.} as the name implies, is both a terminal and computer. It is designed around the S-100 bus structure used in other 8080 microprocessor-based computers and incorporates all of the circuitry needed to perform either function. In essence, Sol combines a central processor unit (CPU) with several S-100 peripheral modules--memory, keyboard input interface (including the keyboard), video display output interface plus audio cassette tape, parallel, and serial input/output (I/O) interfaces. Sol-20 also includes a five-slot backplane board for adding other memory and I/O modules that are compatible with the S-100 bus.

An 8080 microprocessor (the CPU) is the "brain" of the Sol. It controls the functions performed by the other system components, obtains (fetches) instructions stored in memory (the program), accepts (inputs) data, manipulates (processes) data according to the instructions and communicates (outputs) the results to the outside world through an output port. (For information on 8080 operation, refer to the "Intel® 8080 Microcomputer Systems User's Manual.")

As shown in the Sol Simplified Block Diagram on Page X-24 in Section X, data and control signals travel between the CPU and the rest of the Sol over three buses: 1) a 16-line Address Bus, 2) an eight-line Bidirectional Data Bus, and 3) a 28-line Control Bus which is interfaced to the CPU with support logic circuitry. (Note that the use of a bidirectional data bus permits eight lines to do the work of 16, eight input and eight output.) These three buses account for the bulk of the S-100 Bus which connects the Sol to expansion memory and I/O modules.

In the Sol-20, the S-100 Bus structure takes the form of a five-slot backplane board. It consists of a printed circuit board with 100 lines (50 on each side) and five edge connectors on which like-numbered pins are connected from one connector to another. Functionally, the Sol version of the S-100 Bus is comprised of:

1. Sixteen output address lines from the CPU which are input to all external memory and I/O circuitry. (Direct memory access (DMA) devices must generate addresses on these lines for DMA transfers.)
2. Eight data input/output lines that transfer data between external memory and I/O devices and the CPU or DMA devices. (These eight lines are paralleled with eight other bus lines.)
3. Eight status output lines from the CPU support logic: Memory and I/O devices use status signals to obtain information concerning the nature of the CPU cycle. (DMA devices must generate these signals for DMA transfers.)
4. Nine processor command and control lines: Six of these are output signals from the CPU support logic; three of them are input signals to the CPU support logic from memory and I/O devices. (In a DMA transfer, the DMA device assumes control of these lines.)
5. Five disable lines: Four of these are supplied by a DMA device to disable the tri-state drivers on the CPU outputs during DMA transfers. The fifth is a derivative of the DBIN output from the CPU, and it is used to disable any memory addressed in Page ft. Use of this disable is optional with a jumper.
6. Two input lines to the CPU support logic which are used for requesting a wait period. One is used by memory and I/O devices and the other by external devices.
7. Six power supply lines which supply power to expansion modules.
8. Three clock lines.
9. Four special purpose signal lines.
10. Thirty-one unused lines.

Definitions for each S-100 Bus line, as used in the Sol, are provided on Pages AVII-3 through AVII-6 in Appendix VII.

In addition to the S-100 Bus structure, Sol also uses an eight-line keyboard input port, an eight-line parallel input port,

an eight-line parallel output port, an eight-line sense switch logic input port, and a unidirectional eight-line internal data bus.

The use of a unidirectional (input) data bus accommodates Sol's internal low-drive memory and I/O devices that do not meet the heavy drive requirement of the bidirectional data bus. The low-drive requirement of the internal bus also allows using the tri-state capabilities of the UART's (Universal Asynchronous Receiver/Transmitter) in the serial and audio cassette I/O circuits without additional drivers.

All CPU data and address lines are buffered through tri-state drivers to support a larger array of memory and I/O devices than would otherwise be possible with the 8080 output drive capability. Data input to the CPU is selected by a four-input multiplexer from the Keyboard Port, Parallel Port, Bidirectional Data Bus and Internal Data Bus. The Internal Data Bus is the source of all data input to the CPU from Sol's internal memory, the serial interface and the cassette interface. The Bidirectional Data Bus is the source of all data fed to memory and I/O, both internal and external. It is also the source of data input to the CPU from eight internal sense switches as well as from external memory and I/O.

8.3 BLOCK DIAGRAM ANALYSIS, Sol-PC

8.3.1 Functional Elements And Their Relationships

As can be seen in the Sol block diagram on Page X-24 in Section X, timing signals for Sol are derived from a crystal controlled oscillator that produces a "dot clock" frequency of 14.31818 MHz. (This frequency, four times that of the NTSC color burst, provides compatibility with color graphics devices.) The dot clock is applied directly to the Video Display Generator circuit and divided in the Clock Generator to provide $\phi 1$, $\phi 2$ and CLOCK. CLOCK synchronizes all control inputs to the 8080; $\phi 1$ and $\phi 2$ are the nonoverlapping, two phase clocks required by the 8080.

Memory internal to the Sol is divided between 2K of ROM (Read Only Memory), 1K of System RAM (Random Access Read/Write Memory) and 1K of Display RAM. The ROM permanently stores the instructions that direct the CPU's activities. (To enhance Sol's versatility, this particular memory is on a plug-in "personality module". Thus, Sol can be easily optimized for a particular application by plugging in a personality module that contains a software control program designed for the task. The CONSOL and SOLOS programs, which are described in Section IX, are examples of such personality modules.) Display RAM stores data for display on a video monitor, and the System RAM provides temporary storage for programs and data. All memories are addressed on the Address Bus (ADR0-15) and, except for the Display RAM, input data to the CPU on the Internal Data Bus (INT0-7). Data entry into both RAM's is done on the Bidirectional Data Bus (DIO0-7).

As can be seen, Sol's internal memory consists of four contiguous 1024-byte pages. There are two pages (C0 and C4, hexadecimal or hex) of ROM, with Page C0 at hex addresses C000 through C3FF and Page C4 at hex addresses C400 through C7FF. System RAM (Page C8) is at hex addresses C800 through CBFF, and Display RAM (Page CC) is at hex addresses CC00 through CFFF.

The six high order bits of the address are decoded in the Address Page and I/O Port Decoder to supply the required four memory page selection signals. The I/O Port Decoder portion of this circuit decodes the eight high order address bits to provide outputs that control Data Input Multiplexer switching, Data Bus Driver enablement and I/O port selection.

The video display section consists of the Video Display Generator and Display RAM. The RAM is a two-port memory, with the CPU having the higher priority. Screen refresh circuitry in the Video Display Generator controls the second port to call up data as needed for conversion by a character generator ROM into video output signals. Other circuitry generates horizontal and vertical sync and blanking signals as well as cursor and video polarity options.

A 1200 Hz signal, extracted from dot clock by a divider in the Video Display Generator, drives the Baud Rate Generator. This generator supplies the receive and transmit clocks for the serial data interface (SDI/UART) and provides all frequencies required for Baud rates between 75 and 9600. It also supplies clock signals to the Cassette Data Interface (GDI).

A UART controls data flow through the Serial Data Interface (SDI/UART) and provides for compatibility between the Sol and a data communications system, be it RS-232 standard or a 20 ma current loop device. In the transmit mode, parallel data on the Bidirectional Data Bus is converted into serial form for transmission. Received serial data is converted in the receive mode into parallel form for entry into the CPU on the Internal Data Bus. SDI/UART status is also reported to the CPU on the Internal Data Bus. The SDI/UART channel is enabled by the port strobe from the Address Page and I/O Port Decoder.

Circuitry within the GDI derives timing signals from clocks supplied by the Baud Rate Generator. The Cassette Data UART functions to 1) convert parallel data on the Bidirectional Data Bus into serial audio signals for recording on cassette tape, and 2) convert serial audio signals from a cassette recorder into parallel data for entry into the CPU from the Internal Data Bus. Note that Cassette Data UART status is also reported to the CPU on the Internal Data Bus. Again, a UART performs the necessary parallel-to-serial and serial-to-parallel conversions. Other GDI circuitry performs the needed digital-to-audio and audio-to-digital conversions and provides the signals that allow motor control for two recorders. As with the SDI/UART, the Cassette Data UART is enabled by a port strobe from the Address Page and I/O Port Decoder.

Output data from the CPU that is channeled through the Parallel Port (PP) is latched from the Bidirectional Data Bus by the parallel strobe from the Address Page and I/O Port Decoder. This data is made available at P2, the PP connector. Parallel input data (PID0-7) on P2, however, is fed directly to the Data Input Multiplexer for entry into the CPU.

As can be seen, keyboard data (KBD0-7) from J3 is also fed directly to the Data Input Multiplexer. The keyboard data ready flag, though, is input to the CPU on the internal data bus.

The remaining internal source of data input to the CPU is the Sense Switch Logic, with the data being input on the Bidirectional Data Bus. This is an eight-switch Dual Inline Package (DIP) array that lets the CPU read an eight-bit word when it issues the sense switch strobe via the Address Page and I/O Port Decoder. The sense switch data source is available to interact with the user's software.

CPU Support Logic accepts six control outputs from the CPU, status information from the CPU's data bus and control signals from the Control Bus. It controls traffic on the data buses by generating signals to 1) select the type of internal or external device (memory or I/O) that will have bus access and 2) assure that the device properly transfers data with the CPU.

8.3.2 Typical System Operation

Basic Sol system operation is as follows: The CPU fetches an instruction and in accordance with that instruction issues an activity command on the Control Bus, outputs a binary code on the Address Bus to identify the memory location or I/O device that is to be involved in the activity, sends or receives data on the data bus with the selected memory location or I/O device, and upon completion of the activity issues the next activity command.

Let's now look at some typical operating sequences.

Keyboard Data Entry and Display. Assume the "A" and SHIFT keys on the keyboard are pressed. The keyboard circuitry converts the key closures into the 7-bit ASCII (American Standard Code for Information Interchange) code for an "A" {1000001} and sends a keyboard-data-ready status signal to the CPU on the Internal Data Bus. The monitor program in ROM repetitively "looks" for the status signal. When it finds this signal the program enters its keyboard routine and enables the transfer by switching the Data Input Multiplexer to the keyboard bus via the Address Page and I/O Port Decoder.

Following program instructions, the CPU addresses the Display RAM on the Address Bus to determine where the next character is to appear on the screen. It then stores the ASCII code for the "A" at the appropriate location in the Display RAM and adds one to the cursor position in readiness for the next character. (Addressing is

done over the Address Bus; cursor position and the "A" enter the Display RAM on the Bidirectional Data Bus.) The CPU is now finished with the transfer, and will issue the next activity command.

When the refresh control circuitry calls up (addresses) the "A" from the Display RAM, the character generator ROM decodes the ASCII-coded "A" that is input from the Display RAM and generates the "A" dot pattern (see Figure 8-5 and 6) in parallel form. The ROM output is serialized into a video signal and combined with a composite sync signal to provide an Electronic Industries Association (EIA) composite video signal for display on an external video monitor.

SDI/UART Transfer and Display. A data transfer through the SDI/UART is similar to a keyboard entry, but data can be transferred in either direction.

Assume the SDI/UART wants to transfer an "A" from a modem to the CPU for display on a video monitor. The ASCII code for the "A", received in serial form from the modem on the serial data input of the SDI connector (J1), is fed to the SDI/UART. In the receiver section of the UART the serial data is converted into parallel form and placed in the UART's output register. The UART also sends a "received data ready" status signal to the CPU on the Internal Data Bus. When the program in ROM checks and finds the status signal, the program enters the SDI routine, and enables the transfer by switching the Data input Multiplexer to the Internal Data Bus. The "A" enters the CPU on the Internal Data Bus and is sent to the Display RAM on the Bidirectional Data Bus. Operations involved in displaying the "A" are identical to a keyboard entry.

Now assume the CPU wants to send an "A" to the SDI/UART for transmission. The CPU, under program control, sends the SDI/UART status input port strobe via the Address Page and I/O Port Decoder to the UART. In turn, the UART responds with its status on the Internal Data Bus. Assuming the UART is ready to transmit, the CPU places the ASCII code for the "A" on the Bidirectional Data Bus and sends the SDI/UART data output port strobe which loads the Bidirectional Data Bus content into the UART's transmitter section. The "A" is serialized by the UART and sent out the transmitted data pin of J1.

8.4 POWER SUPPLY CIRCUIT DESCRIPTION

Refer to the Sol-REG and Sol-10 or Sol-20 Power Supply Schematics in Section X, Pages X-12, 13 and 14.

The Sol power supply consists of the Sol-REG regulator and either the Sol-10 or Sol-20 power supply components. An 8 V dc unregulated supply in the Sol-20 is the only difference between the two. We will, therefore, describe the complete Sol-10 supply followed by the unregulated 8 V dc supply in the Sol-20.

Fused primary power is applied through S5 to T1 (T2 in the Sol-20). FWB1, a full-wave bridge rectifier, is connected across the 8-volt secondary (green leads). The rectified output is filtered by C8 and applied to the collector of Q1. Q1, a pass transistor, is driven by Q2, with the two connected as a Darlington pair. The output of Q1 is connected to R1 which serves as an overload current sensor.

An overload current (approximately 4 amps) increases the voltage drop across R1. The difference is amplified in one-half of U2 (an operational amplifier) and the output on pin 7 turns Q3 on. Q3 in turn "steals" current from Q1-Q2 and diverts current from the output on pin 1 of U2. This in effect turns the supply off to reduce the current and voltage. Note that the circuit is not a constant current regulator since the current is "folded back" by R6 and R8. The current is reduced to about 1 amp as the output voltage falls to zero.

Divider network R11 and R12, which is returned to -12 volts, senses changes in the output voltage. If the output voltage is 5 volts, the input on pin 2 of U2 is at zero volts. U2 provides a positive output on pin 1 if pin 3 is more positive than pin 2 and a negative output for the opposite condition.

When the output voltage falls below 5 volts, pin 2 of U2 goes more negative than pin 3. This means pin 1 of U2 goes positive to supply more current to the base of Q1. The resulting increase in current to the load causes the output voltage to rise until it stabilizes at 5 volts. Should the output voltage rise above 5 volts, the circuit operates in a reverse manner to lower the voltage.

Protection against a serious over-voltage condition (more than 6 volts) is provided by SCR1, D1, R2, R13, R14 and C8. Zener diode, (D1), with a 5.1 zener voltage, is connected in series with R13 and R2. When the output voltage exceeds about 6 volts, the resulting voltage drop across R2 triggers SCR1 to short the foldback current to ground. Since the overload current circuit is also working, the current through SCR1 is about 1 amp. Once the current is removed, this circuit restores itself to its normal condition; that is, SCR1 turns off. R13, R14 and C8 serve to slightly desensitize the circuit so that it will not respond to small transient voltage spikes.

Bridge rectifier FWB2, connected across the other T1 secondary, supplies +12 and -12 V dc. The positive output of FWB2 is filtered by C5 and regulated by IC regulator U1. The negative output is filtered by C4 and regulated by U3. Shunt diodes D3 and D4 protect U1 and U3 against discharge of C6 and C7 when power is turned off. (Note that should the -12 volt supply short to ground, the +5 volt supply turns off by the action of U2.)

Unregulated -16 and +16 V dc, at 1 amp, from the filtered outputs of FWB2 are made available on terminals X6 and X5. These are not used in the Sol-10, but they are supplied to the backplane board in the Sol-20 to drive S-100 Bus modules.

In the case of the Sol-20, the power transformer (T2) has an additional 8-volt secondary winding and a third bridge rectifier (FWB3) to supply +8 V dc at 8 amps. The output of FWB3 is filtered by C9 and controlled by bleeder resistor R13. Again, this voltage is supplied to the backplane board in the Sol-20.

Sol-20 also includes a cooling fan powered by the AC line voltage.

8.5 Sol-PC CIRCUIT DESCRIPTIONS

8.5.1 CPU and Bus

Refer to the CPU and Bus Schematic in Section X, Page X-15.

A crystal, two inverter sections in U92 and four D flip-flops (U90) and associated logic make up the Clock Generator.

The two U92 sections function as a free-running oscillator that runs at the crystal frequency of 14.31818 MHz. R133 and R134 drive these two sections of U92 into their linear regions, and C61 and C64 provide the required feedback loop through the crystal. U77, a permanently enabled tri-state non-inverting buffer/amplifier, furnishes a high drive capability.

This fundamental clock frequency is fed directly to the Video Display Generator and to the clock inputs of U90. U90 is a four-stage register connected as a ring counter that is reset to zero when power is applied to the Sol. This reset is accomplished with D8, R104 and C39.

The bits contained in the ring counter shift one to the right with every positive-going clock transition, but the output of the last stage is inverted or "flipped" before being fed back to the input. In a simple four-stage "flip-tail" ring counter, the contents would progress from left to right as follows: 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000--on the first through eighth clocks respectively. The hypothetical counter would go through eight states, dividing the clock by eight.

The Sol counter, however, is a modified flip-tail ring counter that can be configured to divide by one of three divisors--5, 6 or 7. This is made possible by using a two-input NAND gate (U91) in the feedback path and three jumper options (no jumper, D-to-C and D-to-E) to alter the feedback path. Let's see how it works.

Sol is normally configured with the D-to-E jumper installed to meet the clock requirements of the 8080A CPU. With this jumper installed, the outputs of the third and fourth U90 stages are applied to pins 9 and 10 of U91. Assuming U90 is reset to zero, pin 8 of U91 is high, and on the first clock pulse the counter contents change to 1000. (Refer to 2.045 MHz Clocks portion of Figure 8-1 on Page VIII-11.) Pin 8 of U91 cannot change until the fourth state (1111), at which time it goes to zero. On the fifth clock pulse the counter changes to 0111. Again, pin 8 of U91 cannot change from zero until one of its inputs changes. As shown in Figure 8-1, the third U90 stage (C) changes on the seventh clock. The counter now stands at 0001, and on the eighth clock the counter flips to 1000 and the count cycle repeats. The pattern is thus 1000, 1100, 1110, 1111, 0111, 0011, 0001. U90 consequently goes through seven states. We have a 3.5-stage counter that divides DOT CLOCK by seven to supply a 2.045 MHz output.

With no jumper installed, pin 10 of U91 is pulled high by R105, and U91 operates as a simple inverter for feeding back the output of the third U90 stage. In effect we have a three-stage counter that operates in a similar manner to that described in the preceding paragraph. It goes through six states (100, 110, 111, 011, 001, 000) to divide DOT CLOCK by six which produces a 2.386 MHz output. The timing for this option is also shown in Figure 8-1.

Let's now put the D-to-C jumper in. The feedback in this case is the NAND combination of the outputs from the second (B) and third (C) U90 stages. This gives us a 2.5-stage counter that divides DOT CLOCK by five. As can be determined from the 2.863 MHz portion of Figure 8-1, the counter has five states with this option, and the count pattern is: 100, 110, 111, 011, 001.

Outputs from U90 are applied to the logic comprised of the remaining three sections in U91. This logic and the A-to-B jumper option permits extracting clock pulses of varying widths and relationships to each other from various points within the counter. We extract two clock signals: $\phi 1$ on pin 6 of U91 and $\phi 2$ on pin 11 of U91. (The ability to select the frequency and pulse width for $\phi 1$ and $\phi 2$ permits the use of either the 8080A, 8080A-1 or 8080A-2 CPU for U105. The "A" version is the slowest speed unit, the "A-2" has an intermediate speed, and the "A-1" is the fastest.) Let's now see how the pulse width of $\phi 1$ and $\phi 2$ are determined.

$\phi 1$ on pin 6 of NAND gate U91 is low only when its two inputs are high, and this happens only when there is a 1 in the second and fourth stages of U90. This occurs during the time between the fourth and sixth fundamental clocks for 2.04 MHz operation--the fourth and fifth clocks for 2.38 MHz and 2.86 MHz. Keeping in mind that the fundamental clock period is 70 nsec, it is readily seen that the low frequency pulse train on pin 6 of U91 has a pulse width of 140 nsec and the two higher frequency pulse trains have a pulse width of 70 nsec. (Refer to Figure 8-1 on Page VIII-11.)

The A-to-B jumper is installed when the 8080A or 8080A-1 CPU is used in the Sol. Note that the output ($\phi 2$) on pin 11 of NAND gate U91 is low only when the output on pin 3 of NOR gate U91 is high. (This section in U91 is actually a two-input NAND gate which is functionally the same as a two-input NOR gate.) Pin 3 of U91, with the A-to-B jumper in, is high when either the second (B) or third (C) U90 stage is at zero. As shown in Figure 8-1, this occurs between the sixth and tenth DOT CLOCKS, or 280 nsec (4×70 nsec), for 2.04 MHz operation. For 2.863 MHz, it occurs between the fifth and eighth DOT CLOCKS for 210 nsec. The section of NAND gate U91 with its output on pin 11 inverts the output on pin 3 of U91 and introduces a slight delay to insure there is no overlap between $\phi 1$ and $\phi 2$.

With the A-to-B jumper out, pin 11 of U91 is low only when the second stage (B) of U90 is at zero. At 2.386 MHz, this occurs between the fifth and eighth DOT CLOCKS for 210 nsec. This configuration is used for the 8080A-2 CPU.

In summary, we have two non-overlapping pulse trains which represent the 01 and 02 clocks required by the 8080 CPU, and the pulse widths of these two clocks vary with frequency as follows:

<u>FREQUENCY</u>	<u>$\phi 1$ PULSE WIDTH</u>	<u>$\phi 2$ PULSE WIDTH</u>	<u>CPU</u>
2.045 MHz	140 nsec	280 nsec	8080A
2.386 MHz	70 nsec	210 nsec	8080A-2
2.863 MHz	70 nsec	210 nsec	8080A-1

$\phi 1$ and $\phi 2$ are applied to S-100 Bus pins 25 and 24 respectively through inverters (U92) and bus drivers (U77). They are also capacitively coupled to pins 2 and 4 respectively of driver U104, the phase clock conditioner.

An additional clock, called CLOCK, is taken from pin 8 of NAND gate U91. It occurs 70 nsec after $\phi 2$. It is used on the Sol-PC and is also made available on S-100 Bus pin 49 as a general 2.04, 2.38 or 2.86 MHz clock signal.

Three J-K flip-flops (U63 and 64) are used to synchronize the READY, RESET and HOLD inputs to the CPU. All three are connected as D-type flip-flops so that their outputs follow their inputs on the low-to-high transition of the clock. The READY flip-flop input on pins 2 and 3 of one section in U63 is either PRDY or XRDY from the S-100 Bus; these are normally pulled high by R34 and R12 respectively. S-100 Bus signal !PRESET, which is normally pulled high by R55, inputs the RESET flip-flop, the other section of U63. The HOLD flip-flop (U64) input is !P_HOLD, normally pulled high by R56, from the S-100 Bus. Pull up resistors R51, R50 and R53 insure that the high states of these three flip-flops are adequate for the CPU.

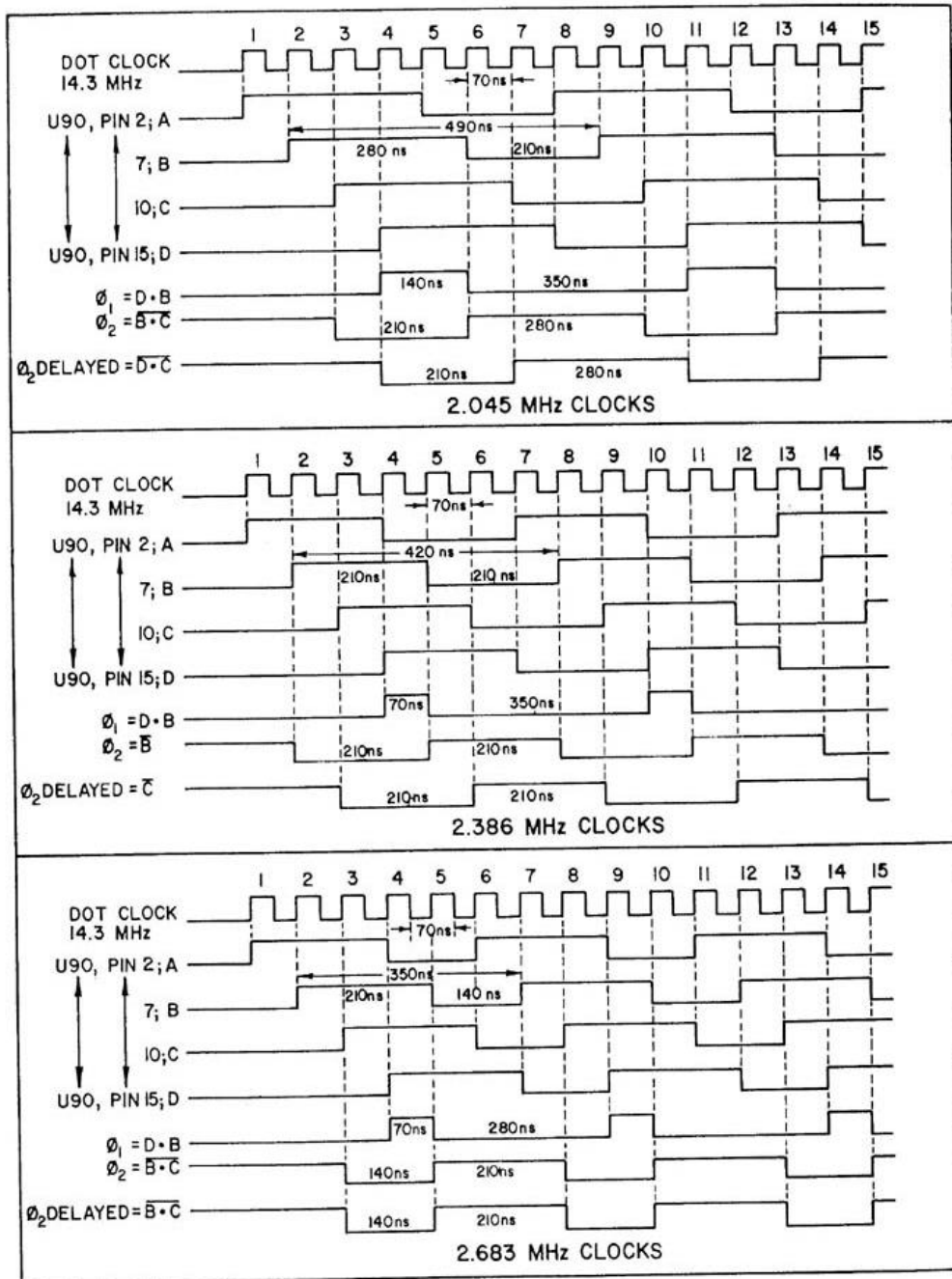


Figure 8-1. CLOCK GENERATOR TIMING

Diode D7, C15 and R18 make up the POC (power on clear) circuit. When power is applied, C15 starts to charge slowly until it reaches the threshold on pin 6 of U46, a Schmitt trigger. (By this time the logic and 5 volt supply have stabilized.) When the threshold is reached, pin 1 of U46 suddenly goes low. The resulting output on pin 8 of inverter U92 is initially low and then rapidly goes high. This signal is passed through a section of U77, a permanently enabled noninverting tri-state driver, as !POC to S-100 Bus pin 99. It is also inverted in a section of U45 to become POC.

The output on pin 8 of U92 is also connected to pin 15 of U63. Thus, pin 9 (RESET) of U63 is high to start the CPU in the reset condition when the Sol is initially turned on.

When !POC goes high, the RESET flip-flop section of U63 is free to clock. Assuming !PRESET is not active, it will change state on the first CLOCK transition. The resulting high on pins 10 and 5 of U63 cause pin 7 (READY) of U63 to go low to place the CPU in the not ready or wait state. This state is subsequently removed on the CLOCK transition following the transition which removed the low from pin 5 of U63. This helps prevent the CPU from starting in a crash condition.

The HOLD flip-flop (U64), however, is not affected by the POC circuit, and was clocked to a low on pin 7 well before the RESET and READY signals became active.

Operation of the POC circuit can also be initiated, without turning the power off, by a keyboard restart signal on pin 13 of J3 or by closing S1-1 if the N-P jumper is in. In either case, C15 is discharged through R58 and then allowed to recharge after !KBD_RESTART is removed or S1-1 is opened.

!POC also resets all stages of D flip-flop U76 (the phantom start-up circuit) to zero. On initial start-up, the CPU performs four fetch machine cycles (refer to Intel® 8080 Microcomputer Systems User's Manual) in accordance with program instructions. For each fetch, the CPU outputs a DBIN on pin 17. U76, connected as a four-stage shift register, is clocked by the inverted DBIN signal on pin 3 of NOR gate U46. Thus, !PHANTOM, on S-100 Bus pin 67, is active low (assuming the F-to-G jumper is in) for the first four fetches or machine cycles. After the fourth DBIN, !PHANTOM goes high. !PHANTOM is used to 1) disable any memory addressed in Page 0 that has Processor Technology's exclusive "Phantom Disable" feature and 2) cause the Sol program memory (ROM), which normally responds to Page C0 (hex) to respond to Page 00 (hex). The second function is discussed in Paragraph 8.5.2.

The inverted DBIN on pin 3 of U46 is also applied to pin 12 of NOR gate U46 and inverted to appear as PDBIN on S-100 Bus pin 78. This section of U46 also allows !DIG1 (bus pin 57) to override DBIN. (!DIG1 is used when an external DMA device replaces the CPU in terms of writing into and reading from memory.) The other CPU control signals (SYNC, INTE, HLDA, WR and WAIT) are also fed to the S-100 Bus pins as indicated. These, as well as DBIN or !DIG1, are placed on the bus through tri-state drivers which are enabled by C/C DSB on S-100 Bus pin 19. Note that this signal is normally pulled high by R20.

The data lines of the CPU (D0-7) are bidirectional and are used for several functions. One of these is to output status at the start of each cycle which is marked by the SYNC output of the CPU. Status on D0-7 is latched in U93 and U106 (each of which contains four D flip-flops) when pin 8 of inverter U45 goes high. Status information, as identified on the schematic, is then buffered through tri-state drivers U94 and U107 to the S-100 Bus. The status latch strobe on pin 8 of U45 is extracted in the middle of the SYNC pulse by gating PSYNC and ! ϕ 2 in NAND gate U44. !STAT_DSB on S-100 Bus pin 18 is used to disable the U94 and U107 buffers when a DMA device or another processor assumes control of the S-100 Bus.

A second function of D0-7 is to output data from the CPU to the Bidirectional Data Bus. Data out of the CPU is placed on this bus through tri-state drivers (U80 and U81). Note that these drivers are normally enabled unless this bus is in the input mode or an external device has control of the bus. In the latter case, !DO_DSB on S-100 Bus pin 23 would be pulled low to make pin 8 of NOR gate U48 high. In the input mode pin 8 of U48 is high because !OUT_DSB is low. This signal is generated by decoding !PAGE_CC, MEM_SEL, !PORT_IN_FC, PORT_IN_FD, INT_SEL to produce MPX_ADR_A and MPX_ADR_B on pins 3 and 11 respectively of two NOR gates in U48. MPX_ADR_A and MPX_ADR_B are decoded with !DBIN on pin 5 of NAND gate U47.

The D0-7 bus lines are also used to input data to the CPU. Data input to the CPU is multiplexed from four data buses with four 4-to-1 line multiplexers (U65, 66, 70 and 79). These four buses are the: 1) Keyboard Data Bus, KDB0-7, 2) Parallel Input Data Bus, PID0-7, 3) Internal Data Bus, INT0-7, and 4) Bidirectional Data Bus, DIO0-7.

These data multiplexers are tri-state devices, with their outputs pulled up by R107 through R114 to a level that satisfies the input requirements of the CPU. Their outputs are active only when both their E1 and E2 (pins 1 and 15) are low. As can be seen, this occurs only when !DBIN on pin 3 of NOR gate U46 is low; that is, when the DBIN output of the CPU is active to indicate its data bus is in the input mode.

Input selection to the multiplexers is done with the A and B inputs to U65, 66, 78 and 79. These two inputs are driven by MPX_ADR_A on pin 3 of NOR gate U48 and MPX_ADR_B on pin II of NOR gate U48. There are four possible states for the combination of MPX_ADR_A and _B, and their relation to input selection is as follows:

1. If both are active (high), the multiplexers select the Bidirectional Data Bus.
2. When the keyboard is called up by the CPU, only !PORT_IN_FC is active (low) to make MPX_ADR_A low. This selects the Keyboard Data Bus.
3. When the parallel port is called up by the CPU, only !PORT_IN_FD is active (low) to make MPX_ADR_B low. This selects the Parallel Input Data Bus.
4. When the CPU selects any I/O port that uses the Internal Data Bus, only !INT_SEL (pin 2 of U47 and U61) is active. Thus, both MPX_ADR_A and _B are low to select the Internal Data Bus.

Two other conditions, defined by !PAGE_CC on pin 2 and MEM_SEL on pin 1 of NAND gate U44, are possible. When any of the four memory pages in the Sol are accessed, MEM_SEL goes high and an inversion in U44 (!PAGE_CC is normally high) appears as a low MPX_ADR_A and _B to select the Internal Data Bus. Should Page CC (the Display RAM) be addressed, !PAGE_CC also goes active (low) to override MEM_SEL. MPX_ADR_A and _B are consequently high to select the Bidirectional Data Bus. These two conditions are required since the ROM and System RAM use the Internal Data Bus and the Display RAM uses the Bidirectional Data Bus.

The address outputs of the CPU (A0-15) are placed on the Address Bus via tri-state drivers (U67, 68 and 81). These drivers are normally enabled since pin 3 of inverter U49 is pulled high by R36. !ADD_DSB on S-100 Bus pin 22 is used to disable the address drivers when a DMA device or another CPU takes over the bus.

A 5.1 volt zener diode, D11, and a divider network composed of R130, 131 and 132 derive -5 V dc from the -12 V dc supply for use by the CPU. Diode D12 and the same divider supply -12 V dc to pin 3 of U104, the phase clock conditioner.

8.5.2 Memory and Decoder

Refer to the Memory and Decoder Schematic in Section X, Page X-16.

The System RAM consists of eight 1K by 1 bit static memory chips, U3 through U10, and it is assigned addresses C800-CBFF (hex). When the CPU wants to write data into memory, it addresses the System RAM on ADR0-15. ADR0-4 select the row inside the RAM chips, ADR5-9 select the column, and ADR10-15 select the page (in this case Page C8, hex). Page selection enables the eight RAM chips on pin 13. For a read operation, MWRITE on S-100 Bus pin 68 is low, and the resulting high on pin 3 (WE) of the RAM chips keeps them in the read mode. Thus, data on the Bidirectional Data Bus is read into the PRAM'S on their D1 (pin 11) inputs. MWRITE is high, however, during the time the CPU wants to write data into memory. In this case, pin 3 of the RAM's is low to enable them to accept data from the Bidirectional Data Bus.

The ROM is also addressed on ADR0-15 as is the System RAM. Since there can be two pages, however, two enable lines (one for Page C0, hex, and the other for C4, hex) are provided. The C0 and C4 enables are connected to pins A6 and A5 respectively of J5, the Personality Module connector. Unlike the RAM, the ROM can only read data into the CPU, so the previously discussed MWRITE signal is not needed. Data out of the ROM is output on the Internal Data Bus on pins A3, A4 and B5-10 of J5.

ADR10-15 are input to the Address Page and Port Decoder (U34, 35, 36 and their associated logic). U34 (Address Page), U35 (Output Port) and U36 (Input Port) are 3-to-8 line decoders which have three enable inputs (G1, G2A and G2B). G1 must be high and both G2A and B must be low in order to obtain an active output.

Let's look at the Address Page Decoder, U34, first. It must be able to decode four pages: C0 and C4 (ROM), C8 (System RAM) and CC (Display RAM). (Note that these are the hexadecimal digits of the six high order address bits, ADR10-15).

The high order four bits (ADR12-15) must be 1100 (C, hex) in all cases by virtue of the U22 exclusive OR logic. If they are not, the G1 enable on U34 is low to disable that decoder. Bits ADR10 and 11 (The A and B inputs to U34) are the high order bits of the second hexadecimal digit which must be 00 (0, hex), 01 (4, hex), 10 (8, hex) or 11 (12, hex) if U34 is to have an active output. For C0, pin 11 of U34 is active (low); for C4, pin 10 is active; for C8 pin 9 is active; and for CC pin 7 is active. These outputs are applied to the appropriate memories and also provide the MEM_SEL signal on pin 6 of one section in U23. (This section is actually a 4-input NAND gate which is functionally the same as a 4-input NOR gate.)

Note that the U22 logic input with ADR14 and 15 is also connected to !PHANTOM. When this signal is active (low), the output on pins 3 and 11 will be low to disable U34 when ADR12-15 represent a C. If Page 0 is addressed, however, pins 3 and 11 of U22 are high, and this, coupled with lows on ADR10-13, are decoded by U34 as an active output on pin 11. The ROM will consequently respond to addresses in Page 0 and C0 (hex) as long as !PHANTOM is active.

The other two enables on U34 (G2A and G2B) are connected to SINP and SOUT. These two status signals indicate an input or output operation during the CPU cycle. U34 is therefore disabled during these operations.

SINP and SOUT are also fed to pins 5 and 6 of NOR gate U53 which detects an input or output operation. Its output is inverted by U54 and applied to pin 9 of another U53 NOR gate. The other input (pin 8) to U53 is MEM_SEL. So during a memory reference, input operation or output operation, pin 10 of U53 is active to enable the PRDY driver, U71. The low on pin 10 of U53 is also clocked by ϕ_2 as a high to pin 7 of U70, a J-!K flip-flop that is connected as a D flip-flop. Note that the $!(PSYNC \ \& \ !\phi_2)$ signal on pin 5 of U70 forces U70 to set during the middle of PSYNC (refer to CPU and Bus discussion). U70 cannot clock until pin 5 is released, and this occurs simultaneously with the low-to-high transition of ϕ_2 . PRDY is thus low immediately after pin 10 of U53 goes low and remains in that state from the middle of PSYNC to the first positive-going ϕ_2 after PSYNC. This is the time the CPU tests the status of the ready lines (PRDY and XRDY). If either is low, the CPU enters a WAIT state. U53, 70 and 71 thus guarantees that the CPU enters one WAIT state during cycles in which an input, output or memory reference is made.

U35 and 36, the Output and Input Port Decoders respectively, decode the higher order eight address bits (ADR8-15).

All Sol ports have a hexadecimal F (1111) in their high order four bits (ADR12-15 are 1's). The second hexadecimal digit is also never less than eight. This means that ADR11 is always 1 for a port address. These five address bits are thus NAND gated in U23 to provide one of the enables on U35 and 36. Note that the ADR14-15 combination is derived from the output on pins 3 and 11 of the U22 exclusive OR logic. This is permissible since no I/O operations are performed during the first four start-up cycles of the CPU.

The A, B, and C inputs to U35 and 36 (ADR8, 9 and 10 respectively) specify the second hexadecimal digit in the port address and are decoded to supply the indicated outputs. These outputs and their functions are defined in Table 8-1. U36 is enabled to decode when PDBIN and SINP are active; that is, during an input operation. U35 is enabled when SOUT and !PWR are active; that is, during an output operation.

INT_SEL on pin 8 of inverter U83 is the remaining signal generated by the Input Port Decoder circuit. This signal is active when either input port F8, F9, FA or FB is decoded by U36.

Both the address page and input/output decoders can be disabled by SINTA (S-100 Bus pin 96) when the AE-to-AC and AB-to-AD jumpers are installed. SINTA is active (high) when the CPU is responding to an interrupt. Should an external device issue addresses during this time, any memory response would interfere with the

Table 8-1. Port Decoder (U35 & U36) Outputs and Their Functions.

PORT DECODER OUTPUT	FUNCTION
!PORT_OUT_FE	Loads starting row address and first display line position information from Bidirectional Data Bus into Video Display scroll circuit.
!PORT_OUT_FD	Clocks data from Bidirectional Data Bus to output data pins of PP connector.
!PORT_OUT_FB	Loads data from Bidirectional Data Bus into Cassette Data UART.
!PORT_OUT_FA	Clocks PP and CDI control bits from Bidirectional Data Bus.
!PORT_OUT_F9	Loads data from Bidirectional Data Bus into SDI UART.
!PORT_OUT_F8	Clocks RTS (request to send) from bit 4 of Bidirectional Data Bus to pin 4 of SDI connector.
!PORT_IN_FF	Permits CPU to read data byte entered from Sense Switches.
!PORT_IN_FE	Places Video Display scroll timer and screen position status on bits 0 and 1 of Bidirectional Data Bus.
!PORT_IN_FD	Switches Data Input Multiplexer to input data pins of PP connector and resets PP at end of a transfer to ready it for another.
!PORT_IN_FC	Switches Data Input Multiplexer to Keyboard Data Bus.
!PORT_IN_FB	Strobes received data in CDI UART to Internal data Bus.
!PORT_IN_FA	Places PP, keyboard and CDI UART status on Internal Data Bus.
!PORT_IN_F9	Strobes received data in SDI UART to Internal Data Bus.
!PORT_IN_F8	Places SDI UART status on Internal Data Bus.

interrupt operation. To prevent this, SINTA is inverted in U58 to 1) disable U34 on pin 6 and 2) force pin 8 of NAND gate U23 high to disable U35 and U36 on pin 5. (This feature is provided to enable future versions of Sol to operate with a vectored interrupt system.)

8.5.3 Input/Output

Refer to the Input/Output Schematic In Section X, Page X-17.

This section in the Sol has five functional circuits: 1) Parallel I/O Logic, 2) Sense Switch Logic, 3) Keyboard Flag Logic, 4) SDI/UART and 5) Baud Rate Generator.

The PP uses U95 and 96 (4-bit D-type registers) and their related logic. Data output to the PP connector (J2) is latched from DIO0-7 by U95 and U96. Data is strobed into these registers on the leading edge of an inverted active !PORT_OUT_FD signal on pin 4 of inverter U54. This strobe is also applied to pin 2 of U73 which functions as a J-K flip-flop that is clocked by ! ϕ 2. When the ! ϕ 2 goes from low to high 200 to 300 nsec after !PORT_OUT_FD, pin 7 of U73 goes low to become !POL on pin 17 of J2. (This delay allows U95 and 96 to stabilize.) U73 is reset in the middle of the following PSYNC which means !POL is active for the balance of the cycle.

The outputs of U95 and 96 are tri-state outputs that are enabled by a low on pin 2. In the absence of POE at pin 15 of J2, pin 2 of U95 and 96 are low by virtue of the output on pin 8 of inverter U55. Note that the input to U55 is normally pulled up through R63. The POE provision permits tri-stating an external bidirectional data bus.

As discussed in Paragraph 8.5.1, parallel input data on J2 is fed directly to the Data Input Multiplexer (see Page X-15). The strobe that indicates the presence of input data, !PDR on pin 4 of J2, is applied to pins 2 and 3 of one section in U72, a J-!K flip-flop which is connected as a D flip-flop. When !PDR goes active (low), pin 7 of U72 will go high on the next low-to-high transition of ϕ 2 to toggle the following U72 stage. At this point pins 9 and 10 of the second section in U72 go high and low respectively. Pin 9 supplies PIAK on pin 5 of J2. When high, PIAK signals the external device that Sol has yet to complete acceptance of the data. The state of pin 10 of U72 is transmitted to INT1 of the Internal Data Bus through a U71 tri-state noninverting buffer. U71 is enabled only for the duration of !PORT_IN_FA (auxiliary status). During the time U71 is enabled, the CPU reads the Internal Data Bus. A high INT1 indicates the parallel input data is not ready; a low indicates the data is ready.

The second U72 flip-flop is preset by !PORT_IN_FD or POC. !PORT_IN_FD is active to read data in from the PP; POC occurs only when Sol is restarted or power is turned on. Thus the PP is reset and ready for another transfer at the end of a transfer or when POC is active.

PXDR on pin 16 of J2 is supplied by the external device. It indicates the device is ready to receive data. !PXDR is buffered to INT2 and will effect the transfer of data to the Internal Data Bus during the status input to the CPU. !PXDR is analogous to the previously discussed PIAK signal.

Sense Switches S2-1 through 8 are driven by !PORT_IN_FF when it is low. Thus, the DIO lines connected to closed switches are driven low, and those connected to open switches are pulled high.

U97 (a 4-bit D-type register) and one section of U52 (a J-!K flip-flop connected as a D flip-flop) latch five bits of data on D103-7 when !PORT_OUT_FA goes active. These bits, which supply the indicated outputs, control conditions in both the PP and CDI. With respect to the PP, PIE enables parallel input, and PUS selects the parallel device for the transfer. The data in these two latches remains until either a new word is read out or POC goes active.

Also during !PORT_OUT_FA, the keyboard flag is reported. !KEYBOARD_DATA_READY on pin 3 of J3 is a low going pulse 1 to 10 usec in duration. It is applied to pin 13 of J-!K flip-flop U70. Some time after pin 13 of U70 goes low, but before 500 nsec, U70 is set by ϕ 2 and pin 10 goes low. This low is buffered through U71 to INT0 to indicate the keyboard is ready to send data. Reset of U70 occurs with a POC or by !PORT_IN_FC. The latter occurs when data is accepted from the keyboard.

The other half of flip-flop U52, with its output on pin 6, latches one bit of status, D104, when !PORT_OUT_F8 is active. Its output is applied to pin 5 of one operational amplifier section in U56 to become the SRTS (request to send) signal on pin 4 of J1, the SDI connector.

The SDI/UART centers around a UART, U51. The UART transmission conditions (parity, word length and stop bits) are determined by the settings of S4-1 through 5. (Refer to Paragraphs 7.5.8 through 7.5.10 in Section VII for descriptions of the switch settings and their effect on transmission.

Data destined to leave Sol through the SDI/UART enters the UART on its TI1-6 inputs from the Bidirectional Data Bus when TBRL (pin 23) is low; that is, when !PORT_OUT_F9 goes active. Circuitry within the UART serializes the input data, which is in parallel form, and outputs it on pin 25 at a rate determined by the clock on pin 40. The binary states at pin 25 are low for a zero and high for a one. Assuming Sol is not in local operation ("off line"), the output on pin 25 of the UART is applied to pins 2 and 11 of J1 via two gates in U55 and the other half of U56.

Data that enters Sol through the SDI/UART on pins 3, 12 or 13 of J1 is input to the SDI UART on pin 20 by way of U38, an inverting level converter that converts data levels of up to 25 volts to TTL levels. (Note that current loop data on pin 12 or 13 of J1 is first rectified before it is applied to U38.) The UART converts this serial data into parallel form and outputs it on R01 through R08 (pins 12 through 5 respectively) to the Internal Data Bus when ROD (pin 4) is low; that is, when !PORT_IN_F9 goes active.

The receive-transmit clock for the SDI UART is supplied by the Baud Rate Generator (U84, U85, U86 and their associated circuitry). U85 is a phase locked loop, U86 is a 7-stage binary counter and U84 is connected as a divide-by-11 counter. The 1200 Hz reference signal applied to pin 14 of U85 is supplied from the Video Display Generator. A phase comparator in U85 compares this signal to the output of a voltage controlled oscillator (VCO) in U85. By feeding an output from U86 (in this case the 1200 Hz output on pin 3) back to the compare input (pin 3) of U85, the circuit acts as a frequency multiplier. The output (pin 4) of U85 remains locked, therefore, to a multiple of its input on pin 14. In this case we have a 128X multiplier to generate 153.6 KHz which is counted down in U86. Since U86 is a 7-stage binary counter, the first stage output (pin 12) is 76.8 KHz (one-half of 153.6 KHz, the clock for U86), the second stage output (pin 11) is 38.4 KHz (one-fourth of 153.6 KHz), the third stage output (pin 9) is 19.2 KHz (one-eighth of 153.6 KHz), and so on to the seventh stage output (pin 3) which is 1.2 KHz (1/128 of 153.6 KHz).

With the exception of outputs on pins 12 and 9, the outputs of U86 are connected to S3, the Baud Rate Switch. The 19.2 KHz output on pin 9 is divided by 11 in U84 to supply 1745 Hz to S3-2. The 38.4 KHz on pin 12 can be connected to S3-8 instead of the 153.6 Hz clock by cutting the L-M connection and installing a jumper between K and M.

Let's now translate the frequencies input to S3 into Baud rates. The Baud rate of a UART is 1/16 of its clock rate. Thus, a 1200 Hz clock equates to a 75 Baud transmission rate, a 1745 Hz clock equates to a 109.1 (110) Baud rate, etc. It is now readily seen that the Baud rate available with S3-8 is 9600 assuming the L-M connection is made (153.6 KHz - 16 = 9600). (The L-M connection is default wired on the Sol-PC; that is, there is a trace between L and M on the circuit board.) If the L-M trace is cut and a jumper is installed between K and M, the Baud rate with S3-8 is 4800 (76.8 KHz - 16 = 4800).

We can thus select any one of eight clock frequencies for the SDI UART with S3, with the highest being determined by the K, L and M jumper arrangement. The selected clock is applied to both the receive and transmit clock inputs (pins 17 and 40 respectively) of the UART. This means, of course, that the UART always receives and transmits at the same Baud Rate.

Returning to the SDI UART, we see that its transmitter output on pin 25 is applied to pin 5 of U55, a two-input NAND gate that is functionally a NOR gate. It is normally enabled on pin 4 by pull-up resistor R44. A low on pin 5 represents a binary 0; a high represents a binary 1. The inverted output on pin 6 of U55 is again inverted (assuming Sol is not operating in Local) by the following U55 NAND gate. One-half of operational amplifier U56, operating open loop, converts TTL levels to RS-232 levels (5 to 15 volts). Pin 3 of U56 is held at +2.5 V dc by the R47 and R48 divider network. When pin 2 is more negative than pin 3, the output on pin 1 of U56, which is fed to pin 2 of J1, is at approximately +10 volts. For the opposite condition, pin 2 of J1 is about -10 volts. Thus, U56 also inverts, and a high or low on pin 2 of J1 represent a binary 1 and 0 respectively.

Two conditions can override transmitted data: a keyboard break (!BRK) or local (!KBD_LOC) command. For a break command, !BRK on pin 4 of J3 and pin 4 of NOR gate U55, is low to hold pin 6 of U55 high for the duration of the !BRK signal. This appears as a "space", or high level, on pin 2 of J1. (A space, or break, condition requires that the space level exist for a period longer than the normal length of a character.) In the case of a !KBD_LOC command from the keyboard, pins 1 and 13 of the other two U55 sections are low. Thus, data cannot be transmitted to pin 3 of NAND gate U55, and pin 11 of NOR gate U55 is held high to enable tri-state driver U37 at pin 15. Data on pin 6 of U55 is consequently looped back by way of U37 and R21 to pin 12 of U38. Data on pin 12 of U38 overrides any data arriving at pin 13 of U38. In local operation, therefore, data from pin 25 of the UART does not appear at pin 2 of J1, but it is looped back to the receiver input (pin 20) of the UART via U37, R21 and U38.

Notice that data on pin 25 of the UART will also be looped back if S4-6 is closed (half duplex operation). But in this case, data from the UART is also fed to pin 2 of J1.

Serial data from the UART that appears at pin 1 of U56 also drives transistor Q1 by way of R45 and R46 to supply the serial current loop output (SCL0) on pin 11 of J1. Q1 supplies 20 ma. (max.) current for a binary 1 and no current for a binary 0.

Pin 23 of J1 (connected through R23 to +12 V dc) is the serial loop current source (SLCS). It can supply up to 20 ma of current to ground and is used when the external current loop device has no current source.

Data received from a current loop device enters Sol on pins 12 and 13 of J1 in the form of no current for a 0 and 20 ma of current for a 1. This input is rectified by bridge rectifier D3-D6 and applied to a light emitting diode (LED) in optical isolator U39. As its name implies, U39 electrically isolates the current loop circuit from the rest of the Sol. (This isolation permits a high offset voltage on pins 12 and 13 of J1.) For a 1, the LED is energized, and

the light is optically coupled to the base of a photo transistor in U39 to cause the transistor to conduct. Conduction translates to a low, or mark, level at the input (pin 13) of U38. Since both the current loop and RS-232 received data (SLR1/SLR2 and SRD respectively) share the input to U38, both should not be used simultaneously.

There are five external control signals in the RS-232 section of the SDI/UART: two are sent to the external device (SRTS and SDTR), and three are received from the device (SCTS, SCD and SDSR).

SRTS on pin 4 of J1 was discussed earlier. SDTR (serial data terminal ready) is simply tied to +12 V dc through R24. This indicates to the external device that Sol is connected to it.

SCTS (serial clear to send), SCD (serial carrier detect) and SDSR (serial data set ready) indicate status of the external device. They enter Sol on pins 5, 8 and 6 of J1 respectively, and all three are active high. Following level conversion and inversion in line receivers U38, data on these lines is gated through noninverting tri-state buffers U37 to the Internal Data Bus when !PORT_IN_F8 is active.

!PORT_IN_F8 also enables five bits of UART status to be reported over the Internal Data Bus. These are PE, FE, OE, DR and TBRE on pins 13, 14, 15, 19 and 22 respectively of the UART. They are defined as follows:

- PE: Parity Error--received parity does not compare to that programmed. (Bit INT2)
- FE: Framing Error--valid stop bit not received when expected. (Bit INT3)
- OE: Overrun Error--CPU did not accept data before it was replaced with additional data. (Bit INT4)
- DR: Data Ready--data received by UART is available when requested. (Bit INT6)
- TBRE: Transmitter Buffer Register Empty--UART is ready to accept another word from the Bidirectional Data Bus. (Bit INT7)

8.5.4 Display Section

An understanding of how characters are formed on the video monitor will help you follow operation of the display section.

The monitor screen can be thought of as a large matrix of small light elements, or dots, that can be turned on and off. In this context the overall video presentation consists of light and dark dots.

In the Sol, the display format is 64 characters maximum per character row, with a maximum of 16 rows per frame (page). Thus, up to 1024 characters can be displayed per page.

A 9x13 (columns by lines) dot area, or character position, is allotted on the monitor screen for each displayed character (see Figures 8-2 and 8-3 on Page VIII-24). Consequently, each character row consisting of sixty-four 9 x 13 dot areas requires 13 horizontal scan lines. To provide spacing between both characters and rows, only 12 dot lines and seven dot columns within the 9 x 13 matrix are used for character display. Only nine of the available 12 dot lines, however, are used for any given character.

Let's take a closer look at how the 9 x 13 dot matrix is used. The first seven dot columns are available for all character displays; the last two are used to provide a space between characters. The first dot line in a character row is always blank to provide a space between character rows. As shown in Figure 8-2, the second through tenth dot lines are available for all upper case (capital) and control characters, all symbol and punctuation marks (except the comma and semicolon), and all lower case characters (except the g, j, p, q and y). As shown in Figure 8-3, dot lines five through 13 are available to display characters that normally extend below the base line--lower case g, j, p, q and y plus the comma and semicolon.

Now that we have a feeling for how characters are formed on the video monitor screen, we will move on to the circuit description.

Refer to Display Section Schematic in Section X, Page X-18.

The 14.31818 MHz DOT_CLOCK, which defines the period of one dot (69.8 nsec) in a character display matrix, controls all timing in the Video Display Generator. DOT_CLOCK is applied to pin 2 of U28, a four-bit binary counter that is preset to count from seven through 15 to divide DOT_CLOCK by nine. Two 1.591 MHz outputs are supplied by U28: LOAD_CLOCK on pin 11 and !CHARACTER_CLOCK on pin 12. Pin 11 is a low-active pulse of one DOT_CLOCK duration. Pin 12 is high for five and low for four DOT_CLOCK periods. Both the LOAD_ and !CHARACTER_CLOCK low-to-high transitions occur synchronously on the same DOT_CLOCK.

!CHARACTER_CLOCK, which defines the period of one character position (628 nsec), is inverted in U49 to become CHARACTER_CLOCK. It performs most of the clocking functions in the Video Display Generator and is made available on pin 4 of J4 for use by external graphic display devices.

CHARACTER_CLOCK is in turn divided in U31 and U33, both of which are presettable four-bit binary counters. Both start at count 3 when pin 8 of NAND gate U47 is low, and together they count 102 CHARACTER_CLOCKS to define horizontal timing at 64 usec (102 x 628 nsec = 64 usec).

CHARACTER ADDRESS*	LINE ADDRESS	SCAN LINE NO.	COLUMN NO.									VIDEO INFORMATION BITS
			1	2	3	4	5	6	7	8	9	
1001001 ↑ ↓ 1001001	1111	1	0	0	0	0	0	0	0	0	0	000000000 (blank)
	0000	2	0	#	#	#	#	#	0	0	0	011111000
	0001	3	0	0	0	#	0	0	0	0	0	000100000
	0010	4	0	0	0	#	0	0	0	0	0	000100000
	0011	5	0	0	0	#	0	0	0	0	0	000100000
	0100	6	0	0	0	#	0	0	0	0	0	000100000
	0101	7	0	0	0	#	0	0	0	0	0	000100000
	0110	8	0	0	0	#	0	0	0	0	0	000100000
	0111	9	0	0	0	#	0	0	0	0	0	000100000
	1000	10	0	#	#	#	#	#	0	0	0	011111000
	1001	11	0	0	0	0	0	0	0	0	0	000000000 (blank)
	1010	12	0	0	0	0	0	0	0	0	0	000000000 (blank)
	1011	13	0	0	0	0	0	0	0	0	0	000000000 (blank)

*7-bit ASCII code for I # = illuminated dot

Figure 8-2. Example of uppercase character (I) display.

CHARACTER ADDRESS*	LINE ADDRESS	SCAN LINE NO.	COLUMN NO.									VIDEO INFORMATION BITS
			1	2	3	4	5	6	7	8	9	
1110000 ↑ ↓ 1110000	1111	1	0	0	0	0	0	0	0	0	0	000000000 (blank)
	0000	2	0	0	0	0	0	0	0	0	0	000000000 (blank)
	0001	3	0	0	0	0	0	0	0	0	0	000000000 (blank)
	0010	4	0	0	0	0	0	0	0	0	0	000000000 (blank)
	0011	5	#	0	#	#	#	0	0	0	0	101110000
	0100	6	#	#	0	0	0	#	0	0	0	110001000
	0101	7	#	0	0	0	0	#	0	0	0	100001000
	0110	8	#	0	0	0	0	#	0	0	0	100001000
	0111	9	#	#	0	0	0	#	0	0	0	110001000
	1000	10	#	0	#	#	#	0	0	0	0	101110000
	1001	11	#	0	0	0	0	0	0	0	0	100000000
	1010	12	#	0	0	0	0	0	0	0	0	100000000
	1011	13	#	0	0	0	0	0	0	0	0	100000000

*7-bit ASCII code for p # = illuminated dot

Figure 8-3. Example of lowercase character (p) display.

As indicated in Figure 8-4 on Page VIII-27, Subgroup Counter U31 and Group Counter U33 are preset to a count of 3 at the start of each horizontal scan line. U31 counts from 3 through 15 (13 character positions) and enables U33 for one count. U31 then counts 0 through 15 and enables U33 for the second count. The sequence continues through four more groups of 16 character positions, and at this point U33 is at its sixth count (a binary 9). Thus, pins 11 and 14 are high at pins 10 and 11 of U47. U31 continues to count from 0, and on the ninth count (a binary 8) pin 9 of U47 goes high. The resulting low on output pin 8 of U47 loads three into U31 and U33, and the cycle repeats. The U31-U33 cycle) from preset, is then 13, 16, 16, 16, 16 and 9 character position counts for a total of 102.

The QD output on pin 11 of U33 is SCAN_ADV, and the QC output on pin 12 is HDISP. SCAN_ADV is used to generate horizontal synchronization signals, and HDISP defines the start of the display portion of the horizontal scan line.

Four outputs from U31 and the two low order outputs of U33 (pins 13 and 14) are input to the Character Address Multiplexer, U30 and U32, which supplies the low order six address bits to the Display RAM (U14 through U21). The second address source for the Display RAM is the Address Bus, bits ADR0-5. Address source selection is controlled by the output on pin 7 of D flip-flop U75. Pin 7 of U75 goes high when !PAGE_CC (the Display RAM) is active and !(PSYNC & ! Φ 2) goes high (which it does in the middle of PSYNC). Pin 7 of U75 remains high for the rest of the memory access cycle.

The preset signal (pin 8 of U47) to U31 and U33 is applied to the Scan Counter (U40) via inverter U87. U40 counts the horizontal scan lines that make up a row of characters and supplies the line number to U25, the Character Generator ROM. (This ROM is discussed later.) U40 is preset to a count of 15 for the first scan line in the character row. It then counts from 0 through 11. On count 11, SCAN_ENABLE on pin 8 of U47 is inverted in U87 to disable the Scan Counter. A decoder, comprised of NAND gates U59 and U60, decodes the 13th count (count 11) in U40 and SCAN_ENABLE to supply a load pulse to pin 9 of U40. This resets U40 to a count of 15, and the cycle repeats. (Presetting the Scan Counter to a count of 15 permits the Character Generator ROM to provide a blank spacer line between character rows since line 15 in the ROM is always blank.)

The output on pin 8 of NAND gate U59, after inversion in U87, becomes the OVERFLOW_LINE signal. This signal occurs after each character row and appears at pins 7 and 10 of Text Counter U62 to enable it to count. Thus, the Text Counter counts character rows. It resets itself with its carry output (pin 15) through another inverter in U87, with the reset count being determined by the state on pin 10 (VDISP) of J-!K flip-flop U43. If VDISP is low, the Text Counter resets to a count of 0; if VDISP is high, it resets to a count of 12.

Assume VDISP is active (low), which it is during the vertical display portion of the displayable area on the screen. (Refer to Figure 8-4.) U62 is then preset to a count of 0 and will count from 0 through 15 (16 character rows). The resulting carry output on count 15 of the Text Counter causes the U43 VDISP flip-flop to toggle. It also appears as a low on the load input of the Text Counter. The Text Counter is also enabled to reset by virtue of the OVERFLOW_LINE going low after the reset of the Scan Counter. Since VDISP is now high, the Text Counter is reset to a count of 12 and will count 12 through 15 (four character rows). The carry output from the Text Counter then causes the U43 VDISP flip-flop to toggle, and the Text Counter is reset to a count of 0. We can now see that the Text Counter counts 16 character rows when the display is active (VDISP is low) and four character rows when the display is blanked (VDISP is high). The total of 20 character rows represents a full display of 260 scan lines for 60 Hz operation (13 scan lines/row x 20 rows = 260 scan lines per page).

Horizontal and vertical synchronization signals are generated by two one-shot multivibrators consisting of three two-input NOR gates in U102. Horizontal sync is triggered by SCAN_ADVANCE and vertical sync by !VDISP. Both circuits generate fixed-length sync pulses with adjustable starting times. C52 determines the length of the horizontal sync pulse and C53 the length of the vertical sync pulse. The starting times, with respect to triggering, are variable with variable resistors VR1 (HORIZ) and VR2 (VERT) to provide continuous adjustment of the display position on the screen. An exclusive OR gate in U74 combines the two sync pulses into a composite sync (COMP_SYNC) signal. Note that the use of the exclusive OR inverts the horizontal sync pulses when the vertical sync pulse appears. Since vertical sync information is extracted in a monitor by an integrating, or averaging, process, this technique maintains horizontal synchronization during the vertical sync period.

Two types of blanking are available: control character blanking and video blanking. The first blanks control characters and causes cursor information to be displayed in their place. Video blanking forces portions of the video display to a white or black level, depending on whether normal or reverse video is selected with S1-4.

Control character blanking, switch selectable with S1-3, is accomplished with one NAND gate in U60 and one NAND gate in U61. When a control character is present in the Data Latch (U26 and U27), pins 3 and 15 of U26 are high. Assuming the blanking option is selected (S1-3 closed), the output of U60 (!LOAD_CLOCK) is gated with the control character bits by U61 to clear the video parallel-to-serial converter, U41. U41 then loads all zeros instead of the character.

Video blanking is initiated by the PRE_BLANK or COMP_BLANK (pin 14 of Blank Latch U42) inputs to U59, a three-input NOR gate. The third input, the video output on pin 6 of exclusive OR gate U74, is blanked when any of the two blanking inputs is active.

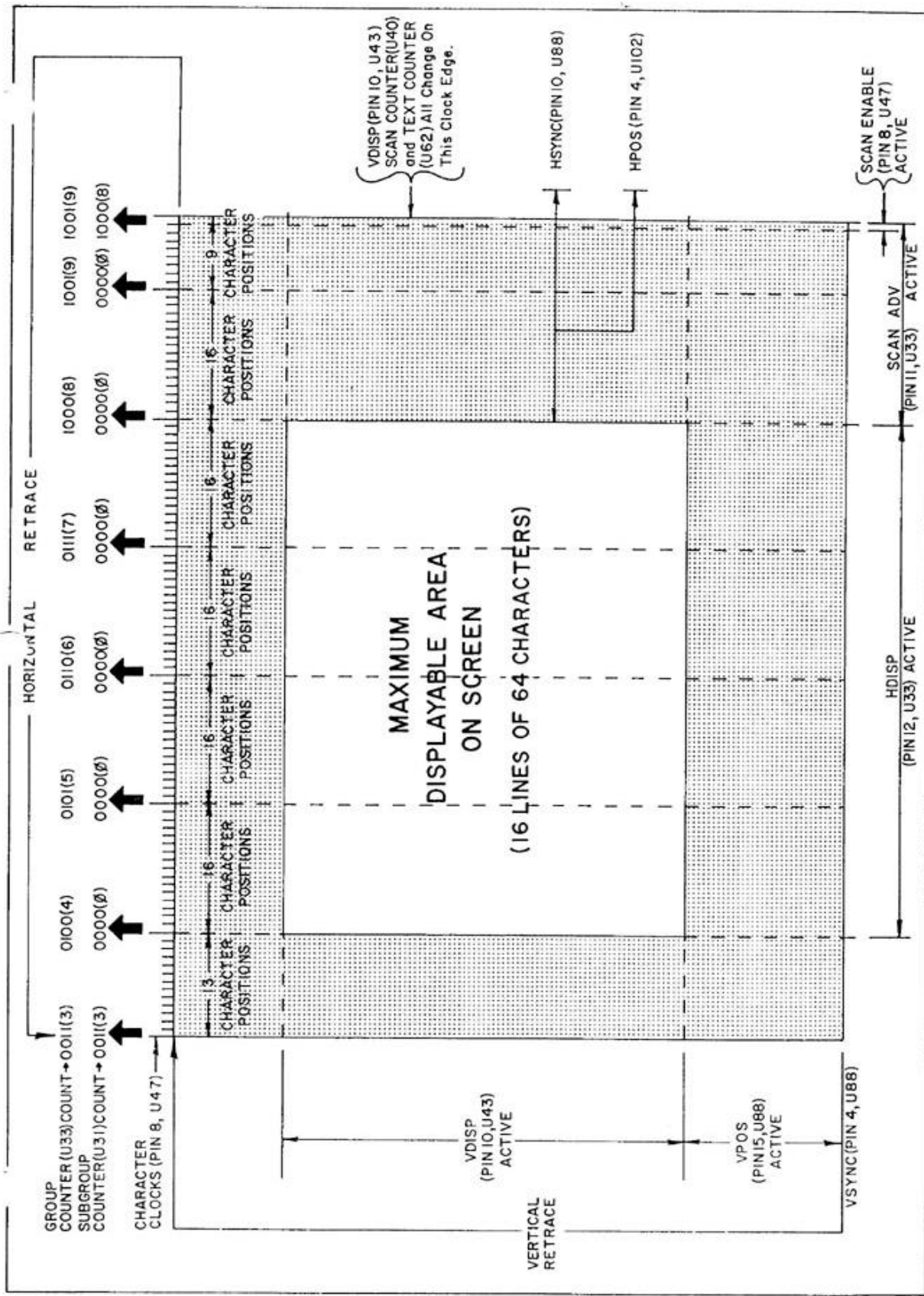


Figure 8-4. VIDEO DISPLAY TIMING

The PRE_BLANK input provides "window shade" blanking which is analogous to pulling a window shade down from the top of the display. PRE_BLANK is generated in one half of J-K flip-flop U43. U43 is reset by the TC output of First Screen Position Counter, U11, and set by VDISP. The output on pin 7 of U11 is generated by the scrolling circuitry (to be discussed later) and defines the character row for which the "window shade" ends. It may begin with any character row from zero through 14.

The remaining video blanking function concerns the output on pin 14 of D flip-flop U42. This signal, COMP_BLANK, is a composite of HDISP and VDISP.

Since there is a two character time delay between Display RAM addressing and the corresponding video output on pin 6 of exclusive OR gate U74, the horizontal and vertical blanking signals must be delayed an equal amount. U42, connected as a two-stage shift register, functions to shift the blanking into synchronization with the video. Since U42 is clocked by LOAD_CLOCK (which has a period equal to one character time), COMP_BLANK is delayed two character times from the input on pin 4 of U42. COMP_BLANK is active low during nondisplayable portions of the video scan to override any video input data on pins 1 and 2 of NOR gate U59. The display is thus blanked.

The Display RAM consists of eight 1K x 1 bit RAM (random access memory) chips, U14 through U28. All chips are held permanently enabled by connecting their CE (pin 13) inputs to ground. Memory addressing is provided through two-to-one multiplexers (U30, U32 and U12) which select one of two display address sources: 1) an external address on Address Bus bits ADR0-9 and 2) an internal address supplied by the Subgroup Counter (U31), Group Counter (U33) and the Beginning Address Counter (U1). The function of the address bits associated with each address source is as follows:

1. External address bits ADR0-5 specify the character position (one of 64) in the character row.
2. External address bits ADR6-9 specify the character row position (one of 16) on the display screen.
3. Internal address bits, a total of six outputs from U31 and U33, specify the character position (one of 64) in the character row.
4. Internal address bits, the four outputs from U1, specify the character row position (one of 16) on the display screen.

Normally the internal display address is multiplexed to the Display RAM. When the CPU or a DMA device requests access (!PAGE_CC active), the multiplexers switch to the external address lines, ADR0-9.

Seven-bit ASCII-coded data is written into RAM chips U14 through U20 from bits DIO0-6 of the Bidirectional Data Bus, and the cursor bit (DIO7) is written into RAM chip U21. This writing occurs when the write enable (WE) input to the RAM chips is low. This occurs when the Display RAM is addressed (!PAGE_CC active low) and MWRITE on S-100 Bus pin 68 is high. The enable is supplied on output pin 8 of NAND gate U44. Data is read out of the Display RAM when pin 8 of U44 is high. Data out of the Display RAM is placed on the Bidirectional Data Bus via tri-state drivers U29 and U89 when !PAGE_CC and PDBIN (S-100 Bus pin 78) are active. U29 and U89 are enabled by a low output on pin 11 of another U44 NAND gate.

Data out of the Display RAM is also strobed into Data Latches U26 and U27 by LOAD_CLOCK. Seven outputs from these latches are used to address the Character Generator ROM, U25. Note that the output from RAM chip U19 is inverted in exclusive OR gate U74 before being applied to the C input (pin 13) of U26, and the complement (pin 14) of the QC output of U26 is used in addressing U25. This is done so that the Data latches will output the space code (0100000) to the Character Generator ROM when the latches are reset. These latches are reset each time !PAGE_CC is active by way of U75, a J-!K flip-flop connected as a D flip-flop, and D flip-flop U42 (Q output pin 6). By outputting the space code on reset, the Data Latches insure a blank character position on the screen.

The Character Generator ROM, U25, has seven character address inputs (A1 through A7), four scan line inputs (RS1 through RS4) and seven data outputs (B1 through B7). It is programmed to generate seven bits (dots) of character information for the selected scan line of the character row. U25 also automatically blanks scan lines that are not a part of the character and shifts the g, j, p, q, y, comma and semicolon to the fifth through 13th scan lines in the dot matrix (refer to Figures 8-2 and 8-3 on Page VIII-24). Complete patterns for the 6574 and 6575 Character Generator ROM's are provided in Figures 8-5 and 8-6 respectively. Note that the address bits A0 through A6 in Figures 8-4 and 8-5 correspond to the A1 through A7 inputs to U25 on the schematic, scan lines R0 through R8 are specified by the RS1 through RS4 inputs to U25 on the schematic, and the data output bits D0 through D6 correspond to the B1 through B7 outputs from U25 on the schematic.

Let's see how the Character Generator ROM produces a character using an uppercase "C" and "T" as an example. In this example, these two characters are to be displayed in the first and second character positions respectively on the third character row of the display screen. Remember that the character position and row parameters are contained in the Display RAM since the 7-bit ASCII-coded

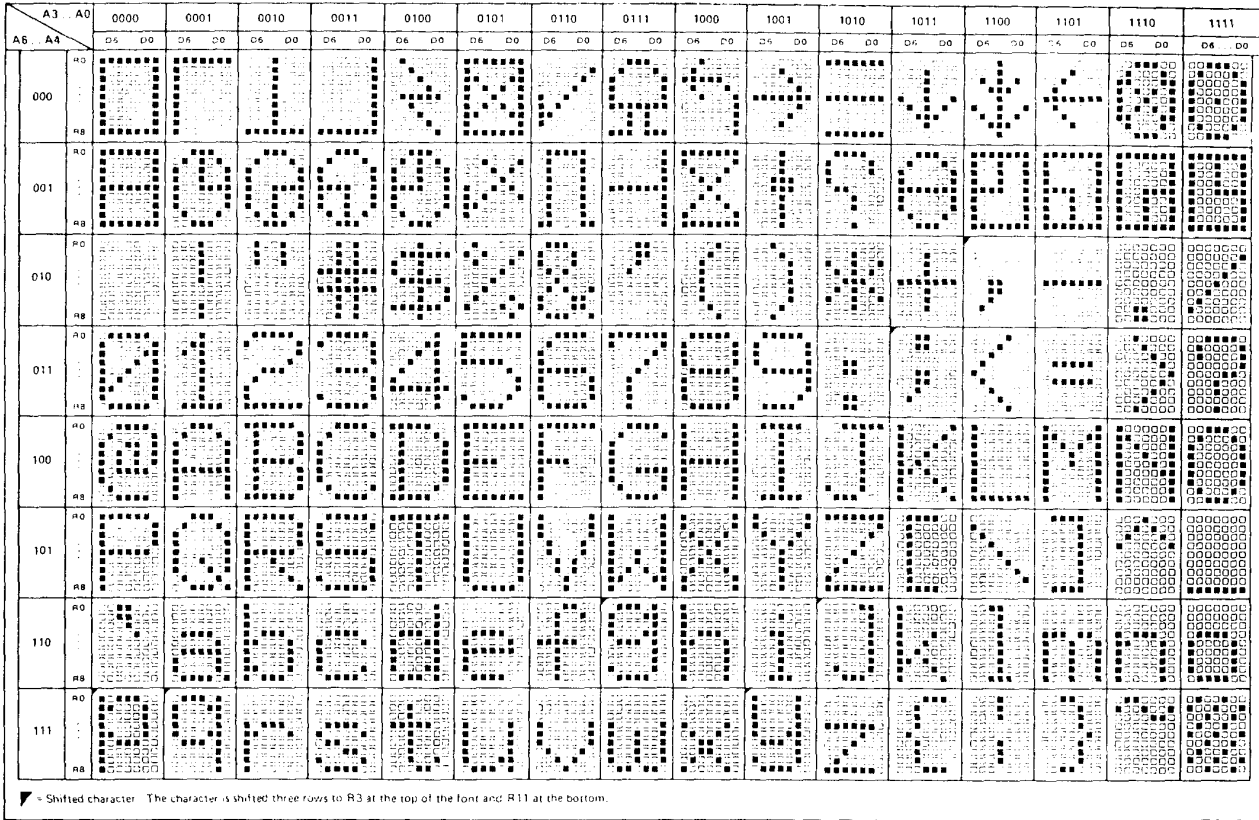


Figure 8-5. 6574 Character Generator ROM pattern.

"C" and "T" were stored in the RAM in the proper character positions in the third character row.

After the first two character rows have been displayed, the Scan Counter (U40) is reset to a binary count of 15 (1111) and the Character and Line Address Multiplexers (U30, U32 and U12) call up the "C" in the Display RAM. The Scan Counter output specifies line 15 in the Character Generator ROM on RSI through RS4. As previously mentioned, this line in the ROM is blank. Thus, the first scan line of the third character row is blank.

The 7-bit ASCII code for the "C" (1000011) is input from the Display RAM to address the Character Generator ROM by way of the Data Latches (U26 and U27). This address is applied to ROM inputs A7 through A1 (A6 through A0 in Figures 8-5 and 8-6). The Scan Counter changes to a count of zero which specifies scan line R0 in the Character Generator ROM. As shown in Figures 8-5 and 8-6, the ROM in turn outputs a 7-bit word, 0011110, on D6 through D0 respectively (B7 through B1 on the schematic).



Figure 8-6. 6575 Character Generator ROM pattern.

For the second character position the Character and Line Address Multiplexers call up the "T" in the Display RAM. The resulting ASCII code for a "T" (1010100) ultimately appears on the address inputs to the Character Generator ROM. Since the Scan Counter is still at a count of zero, the ROM outputs 1111111. This process continues for the balance of the displayable portion of the video scan line.

At the end of the horizontal scan line, the Scan Counter changes to a binary count of 0001 which specifies scan line R1 in the Character Generator ROM. The "C" and "T" are again called up from the Display RAM for the first and second character position respectively. The ROM consequently outputs 0100001 and then 0001000. This sequence continues through scan line R8 when the Scan Counter is at a count of 8 (1000) to produce the "C" and "T".

As discussed earlier, the Scan Counter cycles through 13 counts or scan lines. For the "C" and "T" in our example, the Scan Counter has counted ten lines (15, 0, 1, 2, 3, 4, 5, 6, 7 and 8). The remaining three scan lines are not used in forming the "C" or "T", so on counts 9, 10 and 11 of the Scan Counter the Character

Generator ROM automatically outputs all zeros for these two character positions. After the last scan line in the third character row, the Scan Counter is reset to a count of 15 to start the fourth character row.

The Character Generator ROM output is converted from parallel to serial form in an 8-bit shift register (U41) that is clocked by DOT_CLOCK. For each high bit on the input, the serial output (QH, pin 13) of U41 is high for one DOT_CLOCK period. For each low bit, QH is low for one DOT_CLOCK period. Note that parallel input bit PH (pin 14) is tied to ground. This effectively adds a low bit (or dot) following the data and provides one of the spacer dots between characters. The second spacer dot is generated by connecting the serial input (pin 1) to ground and applying LOAD_CLOCK to the load (LD, pin 15) input to U41. When LOAD_CLOCK goes low, which it does every ninth DOT_CLOCK, U41 shifts in one zero.

A blink oscillator (two inverter sections in U88), a latch (one section in U42) and their associated components comprise the cursor circuit. The blink oscillator runs continuously at a rate set by R84 and C36. Its output has a nominal 0.5 sec period. If the blink option is selected with S1-5, the blink signal is applied to one input of a gate in U60. The other input to this gate is provided by the blink latch, one section in U41. If the cursor bit QA out of Data Latch U26 is high, D flip-flop U42 sets for the time the ROM is active on the character and remains set during the period when video data is shifted out of U41. The output of U42 is gated high through NAND gate U60 when BLINK (pin 6 of U88) is low. BLINK is held low when the blink option is not selected. The output of U60 is in turn gated with the video output of U41 in U74, an exclusive OR gate. U74 thus inverts the video if the output of U60 is high, and no inversion takes place if the output of U60 is low.

The video signal including the cursor, is gated to pin 9 of another U74 exclusive OR gate in the absence of any blanking signals at the other two inputs to NOR gate U59. If S1-4 is open, U74 inverts the video signal to produce a reverse (black on white) display. Raw video on pin 8 of U74 is supplied to pin 15 of J4. Video out on pin 6 of inverter U87 is combined with COMP_SYNC on pin 8 of another U87 inverter in a resistive mixer, R80-R82, to meet EIA composite video signal standards, and coupled to P1 for use by a video monitor. This mixer has a 61-ohm output impedance.

Both Beginning Address Counter U1 and First Screen Position Counter U11 are enabled to advance their counts when pin 9 of J-!K flip-flop U75 is low, which it is for about 600 nsec following !OVERFLOW_LINE; that is, after the Scan Counter (U40) is loaded. This, of course, occurs at the end of every scan line in the character row.

The scroll circuit consists of U1, U11, Scroll Control Latch U2 and Screen Position Control Latch U13 and their associated circuitry. U1 and U11 are up and down counters respectively that are pre-

set to the outputs of latches U2 and U13. U2 latches the starting row address from DIO0-3 and U13 latches the data on DIO4-7, with !PORT_OUT_FE being the strobe. Data on DIO4-7 specifies where the first line will be displayed. Thus, the number loaded into U1 is the address of the first displayable scan line, and the number loaded into U22 defines the character row (0 through 15).

U11 is preset by !VDISP from pin 9 of J-!K flip-flop U43. This means U11 is forced to its preset condition from the end of the displayed text to the top of the next character row. During this time, pin 6 of another U43 J-!K flip-flop is set high to preset U1. If U11 is preset to 0, its TC output on pin 7 is low and pin 6 of U43 is reset to a low. This allows U1 to count with each horizontal scan line.

If U11 is preset to any number other than 0, pin 6 of U43 cannot be reset low until U11 reaches zero. Assume U11 is preset to two. It must count down two character rows before U1 starts counting. During this time, pin 7 of U43 (PRE_BLANK) is low, and as previously discussed, the display is blanked.

We can now see that the PRE_BLANK time, often called "window shade", is variable with the number loaded into U11. Therefore, scrolling is performed by changing the numbers in U2 and U13 without the need to reposition the text within the Display RAM.

The remaining circuit in the Display Section consists of transistor Q2, one section of U87, U89 and U102. U88 and U102 are connected as a one-shot 250 msec timer that is triggered when !PORT_OUT_FE goes active (pin 1 of inverter U87 goes high). Thus, when data is loaded into U2 and U13, this timer starts. Tri-state driver U89, which is enabled by !PORT_IN_FE, transmits the state of this timer to D100 on the Bidirectional Data Bus. The CPU can consequently test the timer status by looking for a high on DIO0. This timing allows a 250 msec scroll rate without the need for complex timing routines in the CPU. Q2, R102 and C37 serve to speed up timer reset.

8.5.5 Audio Tape I/O

Refer to Audio Tape I/O Schematic in Section X, Page X-19.

Timing for the Audio Tape I/O is derived from the 1200, 2400, 4800, 19,200 and 38,400 Hz signals received from the Baud Rate Generator in the Input/Output section of Sol. The first two are used by the write data synchronizer (U100) and the digital-to-audio converter (U101).

The remaining three signals are fed to two sections of U111, a quad multiplexer or select gate. All four sections of U111 are used to select clocks for low speed or high speed operation according to the select inputs, pins 9 (A) and 14 (B). The states of these two select inputs must be complementary to each other in order to select

the high or low speed clocks. Specifically, A must be high and B low to select high speed clocks; the converse condition selects low speed clocks. The select inputs are supplied by TAPE_HI_SPEED and !TAPE_HI_SPEED.

The output of the second section on pin 11 of U111 is BYTE_WRITE_CLOCK, 4800 Hz on low speed and 19.2 KHz on high speed. The third section outputs a 19.2 KHz (high speed) or 38.4 KHz (low speed) timing signal to input pin 10 of binary up counter (U112).

RECOVER_CLOCK is produced by a phase locked loop (U110), another U112 binary up counter and the first and fourth sections of U111. The signal input (pin 14) to U110 is supplied from output pin 1 of D flip-flop U113. It is a constant frequency, regardless of whether one or two transitions are detected in the read data during the count out time (12 counts) of the U112 counter with outputs on pins 13 and 14. A phase comparator in U110 compares the signal input to the output of a voltage controlled oscillator (VCO) in U110 (pin 4). By feeding the VCO output through a counter (the other half of U112) before feeding the counter output back to the compare input (pin 3) of U110, the circuit acts as a frequency multiplier. The output of this circuit remains locked, therefore, to a multiple of the signal input on pin 14 of U110.

The output of U110 is nominally 19.2 KHz. The actual output is determined by the signal input which in turn is a function of tape speed. In other words, the phase lock loop circuit tracks input frequency variations. And it will track such variations within its locking range which is determined by the setting of variable resistor VR3 (connected to pin 12 of U110).

For high speed, the divide-by-four output of U112 (pin 4) is selected as RECOVER_CLOCK. For low speed, the VCO output of U110 is selected for RECOVER_CLOCK. This clock serves as read clock for the CDI UART, U69.

CDI control involves !PORT_IN_FA, !PORT_IN_FB, !PORT_OUT_FB, TAPE_CONTROL_1 and _2, POC (power on clear), TAPE_HIGH_SPEED and !TAPE_HI_SPEED. The last two were previously explained in the discussion of U111. !PORT_IN_FA strobcs the CDI UART status (DR, TBRE, OE and FE--refer to Page VIII-22 for definitions) to the Internal Data Bus, INT3-7. !PORT_IN_FB strobcs received data on pins 5-12 of U69 to the Internal Data Bus, INT0-7. !PORT_OUT_FB loads data from the Bidirectional Data Bus (DIO0-7) into U69. POC simply resets U69 whenever power is applied to the Sol.

TAPE_CONTROL_1 and _2 are used to turn one or two recorder motors on and off. An active low TAPE_CONTROL_1 energizes K1 to close its contacts and turn recorder #1 on; a high de-energizes K1 to turn the recorder off. TAPE_CONTROL_2 does the same thing with K2 to control another recorder. Diodes D13 and 14, which shunt K1 and K2

respectively, prevent damage to the logic circuitry in the Input/Output section due to inductive kickback. R155 and 156 are current limiters that keep the relay contacts from "welding" together.

When the CDI is in the write mode, data is input to the UART (U69) under control of !PORT_OUT_FB. Upon completion of this strobe, the transmit sequence is initiated within the UART, with the transmission rate being governed by BYTE_WRITE_CLOCK.

The transmission sequence begins with a start bit, a low (data zero) on the UART's TO output. It is followed by eight data bits and two stop bits (high on the UART's TO output), with the number of bits being fixed by the connections to pins 34 through 39 of U69.

The data from U69 is applied to the D input of D flip-flop U100 which is clocked at 1200 Hz. Consequently, the output on pin 1 of U100 follows the input data on pin 5 after the rising edge of the 1200 Hz clock. This output is connected to the reset (pin 4) of U101, so when the data out of the UART is high, the first section in U101 is forced to a reset condition. In this condition the J and K inputs to the second stage of U101 are held high which allows the flip-flop to change state on the rising edge of the clock.

The clock for U101 (OUTPUT_CLOCK) is 2400 Hz in the high speed mode or 4800 Hz in the low speed mode. This clock is derived from 2400 Hz in conjunction with the low speed select signal in NAND gate U98 and exclusive-OR gate U99.

In the high speed mode, pins 12 and 13 of U98 are held low, thus holding pin 10 of U98 high. As a result the 2400 Hz signal is inverted in U99 to become the clock for U101.

Pins 12 and 13 of U98 are held high, however, in the low speed mode to enable U98. In this case R117 and C47 provide a delay in the U98 gate. When the 2400 Hz signal on pin 2 of U99 changes state, so does pin 3 of U99. Also, C47 charges through R117 for several usec, at which point pin 10 of U98 is brought to the opposite polarity. The output from U99 then goes high. A series of positive pulses, with a pulse width approximately equal to the R117, C47 time constant (10 usec) and occurring at every transition of the 2400 Hz signal, appears on pin 3 of U99. This circuit thus operates as a frequency doubler in the low speed mode to provide a 4800 Hz clock for U101.

The 2400 Hz signal from which the U101 clocks are derived also produces the 1200 Hz clock signal for U100. As a result the 1200 Hz signal changes state following a propagation delay after the 2400 Hz signal falls.

As previously stated, the second stage of U101 is allowed to change state on the positive going transitions of the OUTPUT_CLOCK as long as the data out of the synchronizer is a "1". The end result is an output on pin 14 of U101 that is one-half the clock frequency (1200 Hz and 2400 Hz in the high and low speed modes respectively).

Assume the data stream out of the UART goes low ("0"). On the next rising edge of the 1200 Hz signal, U100 will reset with Q low and !Q high. A low reset on pin 4 of U101 enables the first U101 stage to toggle on the next rising edge of the OUTPUT_CLOCK which occurs 1/2400 second after the synchronizer output falls. Remember that OUTPUT_CLOCK moves from a low to a high shortly before the 1200 Hz signal did. The reset on pin 4 of U101 is thus removed slightly after the OUTPUT_CLOCK occurred. With the J and K inputs to the first U101 stage high, its output will change state on each succeeding low to high transition of OUTPUT_CLOCK. The second U101 stage in turn can only toggle on the positive going transition of OUTPUT_CLOCK when its J and K inputs are high. Since the inputs are high at one-half the clock rate, by virtue of the first U101 stage, the second U101 stage toggles at one-fourth the OUTPUT_CLOCK rate.

The two sections of U101, therefore, operate as a frequency divider, dividing the OUTPUT_CLOCK by two when the write data is a "1" and by four when the data is a "0". Thus, in the low speed mode, four cycles of the 1200 Hz represent a "0" and eight cycles of 2400 Hz represent a "1". In the high speed mode, one cycle of 1200 Hz represents a "1" and one-half cycle of 600 represents a "0".

The output on pin 14 of U101 is applied to one section in U109 which provides sufficient current drive for the divider network. This divider and a jumper arrangement allow selecting one of three outputs to be fed to the audio output jack J6. The I-to-J jumper selects a 500 mv signal for the auxiliary input to an audio recorder; the I-to-H jumper selects a 50 mv signal for the microphone input to an audio recorder.

When the CDI is in the read mode, data from the recorders enters on J7. This input is fed to the negative input (pin 6) of operational amplifier U108.

The first section of U108 is a high gain amplifier, with its gain (approximately 100) being determined by R142 and R143. The output from this amplifier is coupled to input pin 2 of the following U108 stage and the base of a Darlington pair (Q4 and Q5) which provides high current gain.

Current into the base of transistor Q5 causes C67 to discharge. (C67 charges through R39 to 5 V dc.) The voltage on C67 in turn controls the gate of field effect transistor (FET) Q3. Q3 functions as a variable resistor which can be changed by its gate voltage. Since Q3 is connected between ground and the input network to the

first U108 stage, it serves as a variable shunt. A low gate voltage on Q3 decreases the shunt resistance and the input to U108. In a like manner, a high voltage on C67 results in an increased input to U108. Q3, Q4 and Q5 with their associated circuitry, therefore, serve as an automatic gain control (AGC) circuit which limits the input to the second U108 stage to approximately a positive 2 volt peak signal.

The second stage of U108 is a comparator with hysteresis that performs the needed audio to digital conversion. Feedback resistor R147, in conjunction with R145, establishes the level on the positive input (pin 3) of U108. This level, be it positive or negative, is the threshold voltage, ± 50 mv, which the negative input (pin 2) must exceed in order for the output of U108 to switch levels, positive to negative and the converse. Since the feedback loop is regenerative, U108 switches at its maximum rate, and U108 switches on each transition of the audio signal input. It is in this manner that U108 performs the audio to digital conversion.

The digital output of U108 is inverted in one section of inverter U109 and applied to pin 9 of exclusive OR gate U99 which is connected as a buffer without inversion. If the output of U109 is low, the output on pin 10 of U99 is also low and the output on pin 4 of another U99 exclusive OR gate is high. The voltage across C49 under this condition is minimal. When the output of U109 goes high, C49 starts to charge through R118 until pin 9 of U99 crosses the threshold of that gate. At this point pin 10 of U99 goes high, and since the two inputs to the second exclusive-OR gate are both high, pin 4 of U99 goes low. C49 now discharges because pins 9 and 10 of U99 are at the same level so that the circuit can repeat the operation on the next high to low transition at pin 4 of U109. R118, C49 and U99 consequently serve as a transition detector that produces a pulse less than one microsecond long for each transition of the output on pin 4 of U109, regardless of the polarity of the transition.

Transition pulses from U99 clock both D flip-flops in U113. A transition pulse clocks the top U113 at pin 3 which sets Q (pin 1) high and \bar{Q} (pin 2) low to enable up binary counter U112 on pin 15. Pin 1 is applied to the T) input (pin 9) of the lower U113 and the circuit remains in this state until one of two things occurs: 1) a second transition pulse arrives before U112 reaches count 12 or 2) U112 reaches count 12.

If a second transition pulse arrives before count 12, the bottom U113 stage is set and presents a "1" to the D input (pin 9) of flip-flop U100. This is clocked by the $\bar{!Q}$ output on pin 2 of U113 as a low to pin 12 of U100.

If a transition pulse does not arrive before count 12, the bottom U113 stage outputs a "0" to input pin 9 of U100. On count 12, the C and D outputs of U112 go high to reset U113 by way of U98 at pin 4. As a result the U100 clock goes high, as does pin 12 of

U100. The output on pin 12 of U100 is inverted by U109 and applied to the receive input (pin 20) of the UART.

The Q output on pin 1 of U113, which occurs at the actual bit rate of the incoming data, is also used by the receive clock circuitry to reconstruct the receive clock from the data signal. Received data undergoes serial-to-parallel conversion in the UART and is placed on the R01-8 data outputs of the UART when ROD (pin 4 of the UART) is low (!PORT_IN_FB active) and onto INT0-7. Four status outputs from the UART can also be enabled when SFD (pin 16) is low. These four bits are FE (framing error), OE (overrun error), DR (data ready) and TBRE (transmitter buffer regis-ter empy).

8.6 KEYBOARD

8.6.1 Block Diagram Analysis

A simplified block diagram of the keyboard is provided on Page X-25 in Section X.

The Clock Oscillator produces the basic timing signals for the keyboard, and they are distributed as indicated.

At the heart of the keyboard is a Key Switch Capacitive Matrix which can be viewed as a 16 x 16 X-Y matrix, with X being the column and Y the row. Conceptually, a key depression increases the capacitance between the X and Y coordinates that uniquely define that key.

The Column Scanner supplies a pulse train to the X lines in the matrix, with only one line being pulsed at any given point in time. When a key is depressed to increase the capacitance between the Column Scanner output and a Row Scanner input, the X-Y coordinates for that key are detected to provide an input to the Sense Circuit.

The Sense Circuit in turn generates an input to the Sequence Detector when a key closure occurs. This detector basically detects key closures and count cycles of the Row Scanner to discriminate against false key signals and insure that valid closures are serviced in order.

In the absence of key closures, the Sequence Detector feeds PKD to the Sense Circuit to increase its threshold. This action serves to increase the circuit's noise immunity. On valid key closures, the PKD input is such as to decrease the Sense Circuit's threshold. When valid key closures exist, the Sequence Detector strobes data into the Output Latch. The low order four bits to this latch are supplied by the Row Scanner; the high order four bits are

supplied by the Encoding ROM, with the data being determined by inputs from the Column Scanner and Function Latch Decoder. This strobe (Data Out) also enables the Strobe Generator to output !STROBE a 6 usec pulse that signals the Sol CPU that the Keyboard is ready to send data.

Eight bits of keyboard data (KBD0 through KBD7) are stored in the Output Latch. KBD0 through KBD6 represent the ASCII code for the character associated with the key closure, or closures, that initiated the Data Out strobe from the Sequence Detector. KBD7 is used only for special control characters (e.g. MODE SELECT, CLEAR and cursor movement) that are recognized by the Sol program. The data on KBD0-7 is input to the Sol CPU when it issues !PORT_IN_FC (refer to Paragraph 8.5.2 on Page VIII-14).

The Repeat Counter is enabled when the REPEAT key and a character key in the Key Switch Capacitive Matrix are pressed at the same time. When this occurs, Key Out (initiated by the character key closure) is active, and the Repeat Counter generates a periodic Repeat Strobe. This strobe disables the Sequence Detector and causes the Strobe Generator to output repetitive !STROBE pulses. Column 30 also prevents the Sequence Detector from strobing additional data into the Output Latch.

The Function Latch and Decoder latches and decodes the Low Order Count from the Row Scanner when the "function key" column in the Switch Matrix is selected by the Column Scanner. It then outputs, as appropriate, !LOCAL, !RST and !BRK to J1 and SHIFT/SHIFT_LOCK, UPPER_CASE and CONTROL bits to the Encoding ROM. The latter three supply three of the seven address bits to the ROM which specify the high order four KBD bits (KBD4-7).

All keyboard outputs are supplied to J1 which is connected to J3 on the Sol-PC.

8.6.2 Circuit Description

Refer to the Keyboard schematic in Section X, Page X-23.

Keyboard operation is controlled by a 3 usec clock circuit consisting of NAND gate U7, R7 and C7. U7 is connected as a Schmitt trigger inverter with negative feedback through R7 and C7. The output on pin 11 of U7, a square wave with a 3 usec period, is inverted in U4 (a NAND gate connected as a simple inverter) and applied to the clock input (pin 11) of U8. U8 operates in a toggle mode by virtue of feeding its !Q output on pin 8 to the D input on pin 12. Thus, its output state changes on each clock to produce a 6 usec and an inverted 6 usec clock on pins 9 and 8 respectively.

Each of these outputs is connected to a section of U7 where each is AND'ed with the 3 usec clock. This generates two negative going clocks at pins 8 and 6 of U7. These outputs are called ! ϕ 1 and

ϕ_2 respectively. This circuit thus generates a symmetrical two phase clock, with each phase having a 6 usec period with a 1.5 usec negative going pulse.

ϕ_1 advances the cascaded ripple counter, U5 and 6, in the Column Scanner circuit (U5, U6, NAND gates U4 and decoders U17 and U21). U6 divides ϕ_1 by two on each advance. The output on pin 12 is consequently a square wave with a 12 usec period, the output on pin 9 is a square wave with a 24 usec period, and so on to pin 11 which has a 96 usec period. The output on pin 11 is then divided by two in U5 to provide 192, 384, 760 and 1536 usec periods. We will call these Clock_1 for the 12 usec period, Clock_2 for the 24 usec period, Clock_4 for the 48 usec period, and so on from Clock_8, _16, _32, _64 and _128.

Clocks_16, _32 and _64 are applied to the A, B and C inputs of binary-to-decimal decoders U17 and U21. In order for these decoders to yield outputs, their D inputs (pin 12) must be low. U4 is used to enable one or the other of these inputs, with Clock 128 being the determining factor. When Clock_128 is low, U17 is selected through U4 when ϕ_1 is high at pin 4 of U4. U21 is selected when Clock_128 is high and ϕ_1 is high at pin 13 of U4. By AND'ing ϕ_1 and Clock_128, neither decoder is selected when ϕ_1 is low, the time U5 and U6 count. During this time false binary signals can appear on the outputs of U5 and 6.

The net effect is that only one of the 15 outputs from U17 and 21 will be low, and this low advances on each count advance. The low outputs of U17 and 21 drive the column lines in the key switch matrix.

Clocks_1 through _8 are connected to analog multiplexers U19 and U22. Only one channel from input to output is connected at one time. Note that Clock_8 and \neg Clock_8 from U6 enable U19 and U22 respectively. U19 and U22 (the Row Scanner) thus scan through the 16 rows in the sequence indicated by the numbers contained within the "boxes" of the key switch matrix. An entire scan of the rows is made before the next column is selected by U17 and 21.

We now have U17 and U21 driving the column lines and U19 and U22 testing each row line by connecting it to an input to the Capacitance Key switch (KTC) Detector. These two inputs are normally high at 5 volts. Within the switch matrix there is a small capacitance connected between each column and row line; that is, there is a capacitance associated with each key on the keyboard. When a key is depressed on the keyboard, the capacitance associated with that key increases. When the column and row lines associated with that key are selected, there is a significant voltage difference between the two and the capacitance charges to produce a small negative going spike at the input to the Capacitance Keyswitch Detector.

This detector circuit consists of three transistors, Q7, Q8, and Q9 (connected as a linear amplifier with negative feedback) followed by Q4 and Q2. Q4 and Q2 are large signal amplifiers biased in their cut-off region. The input to the detector is selectively connected to +5 V dc by way of the analog multiplexers (U19 and U22), the row matrix wires, and the 33K resistors. A key depression causes a negative current pulse through R16 to the base of the input amplifier transistor, Q8, which is biased near cut-off. The pulse is then amplified by Q8 with inversion to appear as a positive pulse at the input of Q7. Q7 is an emitter follower circuit which gives a positive pulse at its output, across R18, at a low impedance. This signal is coupled back to the input through transistor Q9, a common base amplifier which has its base clamped to 2.5 V dc by zener diode CR4. When the positive pulse appears at the emitter of Q9, it is amplified without inversion and applied to the input of Q8. Since the original input was a negative pulse, the positive pulse constitutes negative feedback. The output across R18, a positive pulse, is further amplified by pulse amplifier transistor Q4, a common base amplifier that is normally biased off. The output stage Q2 is biased in the cut-off region also, but a sufficient positive pulse from Q4 will cause Q2 to conduct to give a negative pulse output across R12.

Transistors Q1, Q6, Q5 and Q3, represent a second pulse amplifier circuit that is analogous to transistors Q9, Q8, Q7 and Q4 respectively. The output of this second amplifier, which appears at the collector of Q3, is also connected to the base of the output transistor Q2. An input pulse from either U19 or U22 will therefore supply an amplified negative pulse to pin 13 of NOR gate U14.

The !PKD signal through R24 helps to set the threshold at the base of Q4 and Q3. This threshold is normally high when !PKD is high, so the output from Q7 and Q5 has to overcome a higher threshold at the emitter of Q4 and Q3 in order to cause conduction of Q4 and Q3. On the second such pulse on the same count address, !PKD goes low to reduce the threshold at the bases of Q4 and Q3. This sensitizes the circuit, acting as a positive feedback path, and gives an output. Thus two consecutive detections of a key stroke are necessary to give an output. This feature provides noise immunity since a single noise pulse will not pass through the amplifier. The complete key switch matrix is scanned at a very high rate compared to the time it takes to physically press and release a key. Thus a key closure will be detected, even though the key is not held down for any appreciable time.

Two sections of NOR gate U14 are connected as a cross-coupled flip-flop. A low on pin 13 of U14 sets output pin 11 of U14 high, providing that the low is longer than 1.5 usec (which it is when a valid key closure is detected). That is because ! ϕ 1 is applied to pin 9 of U14. ! ϕ 1 effectively prevents switching noise, which is short in duration, from being interpreted as a key closure. The high, let's call it KEY, on pin 11 of U14 will remain until ! ϕ 1 again goes low about 4.5 usec later.

KEY is fed to pin 5 of 8-input NAND gate U25, pin 9 of ROM U20 and pin 1 of NAND gate U27. Let's examine the other inputs to U25.

KEY, as mentioned, is fed to pin 9 of U20 which is a 256 x 4 bit static ROM. Only two bits are used. For each possible row-column combination, there is one storage location in U20. DI1 and DO1 (pins 9 and 11) are the input and output respectively of one bit location; DI2 and DO2 serve the same functions for the other bit location. The row count is applied to A0-4 and the column count is applied to A5-7 to address U20.

When a key closure is detected, the counts are presented to U20 continuously. When the counts change shortly after the falling edge of $\phi 1$, U20 outputs the status of the address that is already stored in the ROM about 1 usec later on pin 10. On the rising edge of $\phi 1$ after the address change, the status on pin 10 is latched in one-half of D flip-flop U26 and presented at output pins 9 and S. About 1.5 usec later the R/W signal on pin 20 of U20 goes low, and the KEY signal on pin 9 enters the specified location in U20. Note that this KEY is related with the new count address. The key stored in U26 represents the preceding address. We consequently call the KEY in U26 "KEY_minus_1", and it is applied to pin 11 of U25.

The remaining inputs to U25 are 1) $\phi 2$ (an inverted $\phi 2$) on pin 12, 2) a repeat strobe signal on pin 4 (supplied by pin 11 of NAND gate U16 which is high without a repeat command), 3) PKD_minus_1 on pin 6 (supplied on pin 3 of U26 which is low if three or more count cycles have occurred since one key closure), and 4) the column output on pin 4 of U17 which is applied to pins 1, 2 and 3. The last signal drives the column associated with the special function keys on the keyboard (SHIFT, SHIFT_LOCK, LOCAL, BREAK, UPPER_CASE, REPEAT and CONTROL).

In order for U25 to output a low on pin 8, therefore, we need a current KEY, a KEY from the preceding count cycle, no repeat function, no drive on pin 4 (column 30, hexadecimal), and we must be on the second count cycle during the current key depression.

With these conditions satisfied output pin 3 of U25 goes low. It is inverted by U10 to a high on pin 11. This signal then clocks the output latches, U1 and 2. On this signal, the data present on the inputs are latched into U1 and 2, and it remains latched until the next output on pin 8 of U25 occurs.

A low on pin 8 of U25 also resets one-half of D flip-flop U11 at pin 13 which causes output pin 9 to go low. On the rising edge of the inverted 6 usec clock from US, the second U11 stage sets and out-

put pin 5 goes low to clear the first stage. The high on output pin 6 is inverted by NAND gate UIO to supply a low active !STROBE on pin 3 of J1. (Note that J1 on the keyboard connects to J3 on the Sol-PC.) The next inverted ϕ 2 clock resets the second U11 stage. We thus have a 6 usec strobe pulse following the latching of data into U1 and U2.

The complement of KEY_minus_1 on output pin 8 of U26 is fed to input pin 10 of NAND gate U16 and is translated to a high on pin 8. The other input on pin 9 is high at this time since it is driven by the signal which indicates the third count cycle. A three-input NAND gate, U27, thus has a high on pin 2. A second input on pin 1 is KEY which is active (high) from the first count cycle of the key closure. The remaining input on pin 13 is supplied by pin 11 of U16, and it is low only when the repeat function is operating. U27 is consequently satisfied and outputs a low on pin 12.

This low appears at pin 5 of NOR gate U16. Pin 4 of U5 is high at this point by virtue of a low on pin 1 of U16 which indicates the third count. Thus, the high on pin 6 of U16 will be stored in the second bit location U20 when ! ϕ 2 goes low at pin 20 of U20. When this happens D02 (pin 12) of U20 goes high to indicate the new status of this bit.

The D02 output is inverted in U10 and applied to input pin 2 of another U26 D flip-flop and to the Capacitance Keyswitch Detector as PKD. PKD serves to lower the detector threshold; that is, the detector offers less "resistance" to its input. This is positive feedback that allows the detector to discriminate between noise and a key closure. Note that two key closures are required before the detector threshold is lowered.

The inverted D02 output from U20 also appears at the D input (pin 2) of U26. Since this flip flop is clocked by ! ϕ 1, the prior status of !PKD, called "!PKD_minus_1", is already present in this latch on output pin 5. If we are on the second count cycle of a key closure, pin 5 is high. If we are on the third count or more, it is low to inhibit U25. As previously mentioned, !PKD_minus_1 is also connected to the NOR gate (U16) used to feed data to pin 11 of U20 from KEY_minus_1.

When the current KEY signal is released, pin 12 of NAND gate U27 and pin 5 of NAND gate U16 go high. The U16 NAND gate that inputs to pin 4 of U16 looks at KEY_minus_1 on pin 2 and the complement of !PKD_minus_1 on pin 1. Thus, pin 1 is high for the first one and a half counts and pin 2 is high for the first count. Upon release of KEY, therefore, pin 3 of U16 is low for the first count. On the second count, KEY_minus_I goes low--as do pin 6 of U16 and pin 12 of U20. On the next ! ϕ 2 clock, the data is read into U20. The output on pin 12 of U20 changes to remove !PKD which increases the Capacitance Keyswitch Detector threshold for greater noise immunity. It also sets !PKD_minus_1 on pin 5 of U26 on the third count cycle

following release of KEY. On the third cycle the circuit reverts to its original state.

This circuit, comprised of U20, U26, U16 and U17 serves two functions. By requiring two events during two consecutive count cycles before generating a KEY, it discriminates against false key closures. It also insures that multiple key strokes are serviced in order. (This is the n-key rollover feature.) That is because the row-column addresses are continuously presented to U20 and this circuit's cycle can occur for each possible key closure. U20 can thus contain data for all possible key closures, and the data will enter U1 and U2 on the KEY generated for each closure as the row-column count progresses.

The previously mentioned column 30 output on pin 4 of U17 drives the keyboard control key "switches". Data for these key closures, present on pins 1, 2 and 3 of addressable latch U12 is latched in U12 during Clock 8 and $\phi 2$ when column 30 is driven. Pin 13 of U12 is connected to the complement of PKD_minus_1. Thus, the data (active low) is strobed into U12 on the first count cycle. During the third count it will be strobed again and a high is read in. When the key is released, a low is strobed in again. As a result, a high active pulse appears on the output line related to the key that was closed for the duration of the key closure.

SHIFT and SHIFT_LOCK, on pins 11 and 10 respectively, are applied through U23 inverter stages to NOR gates U13 and U14. These are connected as a cross-coupled flip-flop. An active SHIFT sets this flip-flop at pin 5 of U13 to make output pin 6 of U13 and output pin 3 of U14 high. The latter is connected to pin 3 of U18, a 512 x 4 bit ROM. U18 is programmed to output the high-order four bits of the data to U1 according to the states of pins 1, 2 or 3.

The U13-14 flip-flop is set to a high on pin 6 if SHIFT_LOCK is active. As can be seen, the shift bit to U18 is high by virtue of the low on pin 6 of U13 and it will remain so until SHIFT again causes U13-14 to change state. When output pin 6 of U14 is high, pin 12 of U24 is low to turn light emitting diode LED1 on. This LED is located in the SHIFT_LOCK key and indicates the keyboard is in a locked shift condition.

When UPPER_CASE is active, pin 7 of U12 goes high to clock D flip-flop U15 on pin 3. This flip-flop is connected to operate in a toggle mode. On the UPPER_CASE "clock", pin 5 of U15 goes to make pin 2 of U18 low. The high on pin 6 of U15 is inverted by U24 to turn on LED2. LED2 is located in the UPPER CASE key. A second closure of this key toggles U15 to the opposite condition.

Now assume the LOCAL key is depressed, the output on pin 5 of U12 goes active high to clock the other D flip-flop U15 stage at pin 11. This stage also operates as a toggle, and output pin 9 goes low to become LOCAL on pin 14 of J1. Again, the high on output pin 8

causes LED3, the LOCAL light, to turn on. A second closure of the LOCAL key toggles this section of U15 to the opposite condition. Note that LOCAL has no affect on keyboard data.

The other outputs from U12 are BREAK (pin 12), CONTROL (pin 6) and REPEAT (pin 9). BREAK is inverted in U23 to become !BRK on pin 4 of J1. CONTROL is applied directly to input pin 1 of U18 so that the control character related to the low order bits enters U1 and U2.

REPEAT is applied to pins 10 and 11 of NAND gate U27 and pin 13 of NAND gate U16. The input to U27 is gated with UPPER_CASE to generate !RST at pin 13 of J1. This means, of course, that REPEAT and UPPER_CASE must be depressed at the same time to generate !RST.

On pin 13 of U16, REPEAT enables that gate so that U16 transmits the output on pin 9 of U9. U9 is connected as a two-stage shift register whose input (pin 2) is ground. It is clocked by clock_128 from U5.

U9 is initially set with output pins 5 and 9 high during the third count cycle by PKD_minus_1. This is also the time when U12 outputs data. If the key is released, U9 clears to a low on pin 9 five count cycles following KEY. If the key is held down, U9 cannot shift since PKD minus 1 remains on preset input pins 4 and 10.

When REPEAT exists at pin 13 of U16, pin 11 of U16 is low to inhibit U25 and U27 at pin 13. This prevents further KEY signals and disables the n-key rollover circuitry. The low on pin 11 of U16 is also inverted by open collector inverter U24 to enable the repeat oscillator (timer U3, R4, R5 and C3). U3 generates a square wave on pin 3 with a period determined by the RC network.

This clocks the first stage of D flip-flop U11, the !STROBE generator, and U11 produces the previously discussed 6 usec !STROBE. U11 continues to generate !STROBE at the repeat oscillator rate until either the REPEAT or character key is released. And with each !STROBE, of course, the data associated with the character key is latched into U1 and U2.

Eight ASCII-coded data bits are output by U1 and U2 to J1 as indicated. Seven bits (0-6) are used for ASCII characters, and the eighth bit (7) is set only for certain control characters that are recognized by the Sol program. These are used for control functions such as MODE_SELECT and cursor movement.

The remaining circuit, R32 and C14, initializes the keyboard when power is applied. That is, it resets the output latches and the SHIFT/SHIFT_LOCK, UPPER_CASE and LOCAL flip-flops. It also inhibits STROBE at pin 1 of NAND gate U10.

