4KRA STATIC READ/WRITE MEMORY MODULE

ASSEMBLY and TEST INSTRUCTIONS

Processor Technology

6200 Hollis Street
Emeryville, CA 94608
Phone: (415) 652-8080

SECTION I

INTRODUCTION and GENERAL INFORMATION

4KRA STATIC READ/WRITE MEMORY MODULE

1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the 4KRA Static Read/Write Memory Module. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components listed in the "Parts List" (Table 2-1) in Section II. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from poor soldering, backward installed components, and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 4KRA Memory Description

The 4KRA Static Read/Write Memory Module has a capacity of 4096 eight bit bytes and operates in a static mode. As opposed to dynamic memories, the 4KRA needs only one power supply and does not require periodic refreshing.

Maximum worst case access time for the 4KRA is 520 nsec. Thus, in any 8080 system, this memory will operate at the same speed as any other memory with an access time between 50 and 520 nsec. Both the access time and non-refresh features of the 4KRA mean no computer "waiting" time is required.

The 4KRA Memory is plug-in compatible with the Altair 8800 bus. It requires +7.5 to +10 Vdc at 1.0 amp (max.) operating power. In addition, the low power memory IC's used on the module can operate in a low power (+1.6 to +2.5 Vdc at 0.5 amp max.) standby mode. Data loss from the 4KRA during loss-of-power or power interrupt conditions can consequently be prevented by using two "D" size batteries for standby power. Provisions for easily adding this standby capability are incorporated in the module design.

1.2.2 Receiving Inspection

When your module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology should it become necessary to do so.) If your 4KRA kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, the parts supplied with the module, as well as the assembled module, are warranted against defects in materials and workmanship for a period of 6 months after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (e.g. DM8131) and/or a complete description (e.g., 6.8 ohm, ½ watt, 5% resistor).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the module to Processor Technology, first obtain authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the module, proceed as follows:

1. Write a description of the problem.
2. Pack the module with the description in a container suitable to the method of shipment.
3. Ship prepaid to Processor Technology, 6200 Hollis Street, Emeryville, CA 94608.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

SECTION II

ASSEMBLY

4KRA STATIC READ/WRITE MEMORY MODULE

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2.1 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1, Page II-2). If you have difficulty in identifying any parts by sight, refer to Figure 2-1 on Page II-3.

2.2 ASSEMBLY TIPS

1. Scan Sections II and III in their entirety before you start to assemble your 4KRA Memory Module.

2. In assembling your 4KRA, you will be following a step-by-step assembly procedure. Follow the instructions in the order given.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or component.

4. When installing components, make use of the assembly aids that are incorporated on the 4KRA PC board and the assembly drawing: (These aids are designed to assist you in correctly installing the components.)

   a. The circuit reference (R3, C10 and IC20, for example) for each component is silk screened on the PC board near the location of its installation.

   b. Both the circuit reference and value or nomenclature (1.5K and 7400, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that the color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5).

6. Install disc capacitors as close to the board as possible.

7. Should you encounter any problem during assembly, call on us for help if needed.

2.3 ASSEMBLY PRECAUTIONS

2.3.1 Handling MOS Integrated Circuits

The memory ICs used in the 4KRA are MOS devices. They can be damaged by static electricity discharge. Always handle MOS ICs so that no discharge will flow through the IC. Also, avoid unnecessary handling and wear cotton--rather than synthetic--clothing when handling these ICs.

Table 2-1. 4KRA Static Read/Write Memory Module Parts List.

INTEGRATED CIRCUITS

1	7400 or 74LS00 (IC35)	1	74LS136 (IC34)
1	74LS05 (IC33)	2	74367, 8097 or 8T97 (IC37, 38)
1	74LS13 (IC36)	1	8836 or 8T380 (IC39)
1	74LS132 (IC41)	32	91L02A or 21L02B (IC1 through 32)

REGULATORS

1	340T-5.0 or 7805UC (IC42)

DIODES

3	1N4001 (D3, 4 and 5)
2	1N270 (D1 and 2)

RESISTORS

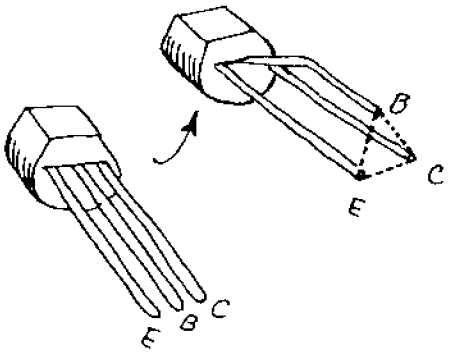
1	39 ohm, 2 watt, 5%
2	470 ohm, ¼ watt, 5%
11	1.5K ohm, ¼ watt, 5% or 2.2K ohm, ¼ watt, 5%

CAPACITORS

23	.1 ufd, disc ceramic
1	1 ufd, tantalum dipped
1	15 ufd, tantalum dipped

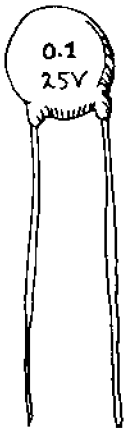
MISCELLANEOUS

1	4KRA PC Board	8	Augat Pins on Carrier
1	Heat Sink	1	Length #24 Bare Wire
1	4 to 7 Position DIP Switch	3	6-32 Screws
6	14-pin DIP Socket	3	6-32 Lockwashers
34	16-pin DIP Socket	3	6-32 Nuts
1	Right Angle Molex Connector, Male	1	Length Solder
1	Mating Connector for Above, Female	1	Manual

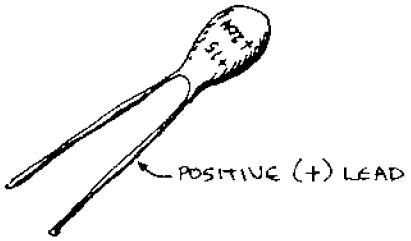


transistor - TO-92 package (plastic)

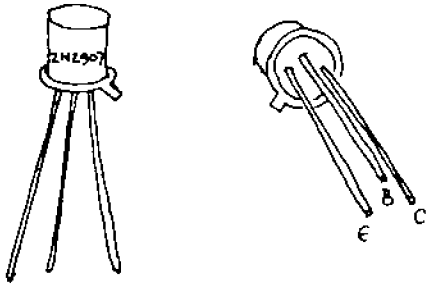
transistor - TO-18 package (metal can)

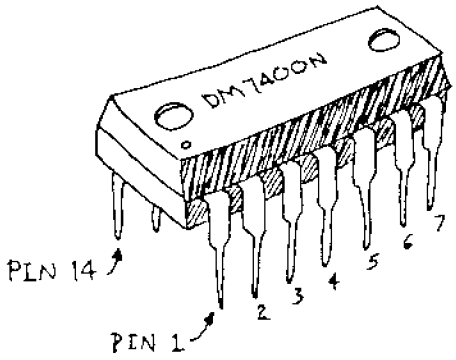


ceramic disc capacitor

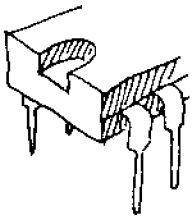


dipped tantalum electrolytic capacitor





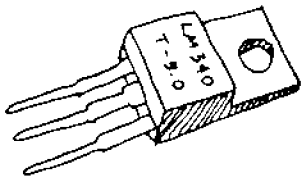
carbon film resistor 5% (gold) or 10% (silver)



NOTE: PIN 1 MAY BE INDICATED BY CORNER DOT OR CUT-OUT.

dual-inline-package (DIP) integrated circuit
8,14,16,24 or 40 pins (14 pin shown)

metal film 1% precision resistor



regulator IC or power transistor (TO-220)

Figure 2-1. Identification of components.

2.3.2 Soldering ** IMPORTANT **

1. Use a low-wattage iron, 25 watts maximum.

2. Solder neatly and quickly as possible.

3. DO NOT press top of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.

4. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.

5. The 4KRA uses a circuit board with plated-through holes. Solder flow through to the component (front) side of the board can produce solder bridges. Check for such bridges after each installation.

6. The 4KRA circuit board has an integral solder mask (a lacquer coating) that shields selected areas on the board. This mask minimizes the chances of creating solder shorts during assembly.

7. Additional pointers on soldering are provided in Appendix III of this manual.

2.3.3 Installing and Removing 4KRA

NEVER install the 4KRA in, or remove it from, the computer with the power on. To do so can damage the board.

2.3.4 Installing and Removing Integrated Circuits.

NEVER install or remove integrated circuits with power applied to the 4KRA.

2.3.5 Use of Clip Leads

NEVER attach clip leads to the top edge of card when power is applied to the 4KRA. To do so will short the +8 Vdc bus to ground.

2.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the 4KRA Memory:

1. Needle nose pliers

2. Diagonal cutters

3. Controlled heat soldering iron, 25 watts

4. 60-40 rosin-core solder (supplied)

5. Volt-ohm meter

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper righthand corner of the board when the edge connector is positioned at the bottom of the board. In this position, the component (front) side of the board is facing up. (Note that the words "COMPONENT SIDE" are silk screened on the component side of the board.) Subsequent position references assume this orientation.

2.6 ASSEMBLY PROCEDURE

Refer to assembly drawing in Section V.

CAUTION

THIS DEVICE USES MOS MEMORY INTEGRATED CIRCUITS (IC1 - 32) WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE THESE ICs SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON, RATHER THAN SYNTHETIC, CLOTHING WHEN HANDLING THESE ICs. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY ENVIRONMENTS.)

( ) Step 1. Check circuit board to insure that there are no shorts between the memory chip mounting pads and that neither the +8-volt bus nor the +5-volt bus are shorted to ground. Using an ohmmeter on its lowest scale, make the following measurements:

( ) 8-volt Bus Test. Measure between edge connector pin 1 or 51 (left end of connector) and pin 50 or 100 (right end of connector). There should be no continuity.

( ) 5-volt Bus Test. Measure between positive mounting pad for C3 and pin 50 or 100 of edge connector. There should be no continuity.

( ) RAM Area Test. Measure between ground (edge connector pin 50 or 100) and each mounting pad (excluding pad 9 which is connected to ground) for IC1. Also measure between +5-volt bus (positive mounting pad for C3) and each mounting pad (excluding pad 10 which is connected to +5 volts) for IC1. Then measure between all combinations of vertically and horizontally adjacent pads for IC1. There should be no continuity in any of these measurements.

If you measure continuity in any of the preceding tests, the PC board is defective and should be returned to Processor Technology for replacement. If none of the measurements show continuity, proceed to Step 2.

( ) Step 2. Install RAM DIP sockets and check installations. Install these sockets in the indicated locations with their end notches oriented as shown on the assembly drawing. Take care not to create solder bridges between the pins and/or traces. (Note that after each column of sockets--e.g., IC8,16,24 & 32 and IC1,9,17 & 25--is installed, you will be testing for any solder bridges (shorts) you may have created.)

( ) IC8,16,24 and 32. Install 16-pin DIP sockets in locations IC8,16,24 and 32. Then make the "RAM Area Test" described in Step 1 of the Assembly Procedure. Make the measurements at IC8. If any of the tests fail, you created a solder bridge at one or more points in the column of sockets just installed. Find and eliminate the short(s) before proceeding further. If your installations pass the tests, continue on to the next column.

( ) IC7,15,23 and 31. Install 16-pin DIP sockets in locations IC7,15,23 and 31. Check this column as you did IC8,16,24 and 32, but make the measurements at IC7.

( ) IC6,14,22 and 30. Install 16-pin DIP sockets in locations IC6,14,22 and 30. Check this column as you did IC8,16,24 and 32, but make the measurements at IC6.

( ) IC5,13,21 and 29. Install 16-pin DIP sockets in locations IC5,13,21 and 29. Check this column as you did IC8,16,24 and 32, but make the measurements at IC5.

( ) IC4,12,20 and 28. Install 16-pin DIP sockets in locations IC4,12,20 and 28. Check this column as you did IC8,16,24 and 32, but make the measurements at IC4.

( ) IC3,11,19 and 27. Install 16-pin DIP sockets in locations IC3,11,19 and 27. Check this column as you did IC8,16,24 and 32, but make the measurements at IC3.

( ) IC2,10,18 and 26. Install 16-pin DIP sockets in locations IC2,10,18 and 26. Check this column as you did IC8,16,24 and 32, but make the measurements at IC2.

( ) IC1,9,17 and 25. Install 16-pin DIP sockets in locations IC1,9,17 and 25. Check this column as you did IC8,16,24 and 32, but make the measurements at IC1.

After installing the sockets for IC1 through 32 and checking your installations for freedom from solder bridges, proceed to Step 3.

( ) Step 3. Install remaining DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the assembly drawing. Take care not to create solder bridges between the pins and/or traces.

LOCATION	SOCKET TYPE
( ) IC33	14 pin
( ) IC34	14 pin
( ) IC35	14 pin
( ) IC36	14 pin
( ) IC37	16 pin
( ) IC38	16 pin
( ) IC39	14 pin
( ) IC40*	None*
( ) IC41	14 pin

*This location is for the "wait state counter" which is not required since the 4KRA runs at maximum speed. Thus, IC40 is not supplied with your kit. For special applications a 74LS109, which needs a 16-pin socket, can be installed in this location.

( ) Step 4. Install heat sink. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the triangle of mounting holes is under one of the triangular cut-outs in the sink. Using two 6-32 screws, lockwashers and nuts, attach heat sink to board. Insert screws from back (solder) side of board. (Refer to Figure 2-2 on Page II-8.)

( ) Step 5. Install IC42 (340T-5.0 or 7805UC). Position IC42 on heat sink and observe how the leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent downwards at a point approximately 0.2 inches further from the body than the other leads. Bend the leads so that no contact is made with the heat sink when IC42 is flat against the sink and its mounting hole is aligned with the hole in the sink. Fasten IC42 to sink using 6-32 screw, lockwasher and nut. Insert screw from back (solder) side of board. Solder and trim leads. (Refer to Figure 2-2.)

( ) Step 6. Install male Molex right angle connector in its location directly below the heat sink. Position connector with pin 1 at top, insert leads in mounting holes, solder and trim.

( ) Step 7. Install diodes D1 and D2 (1N270) in their locations in the lower left corner. Position D1 so that its dark band

mark (cathode) is at the bottom, and position D2 so that its dark band mark is on the righthand side. Solder and trim leads.

( ) Step 8. Install diodes D3, D4 and D5 (1N4001) in their locations on the middle righthand side of the board. Position D3 and D5 so that their dark band marks (cathode) are at the top, and position D4 so its dark band is at the bottom.

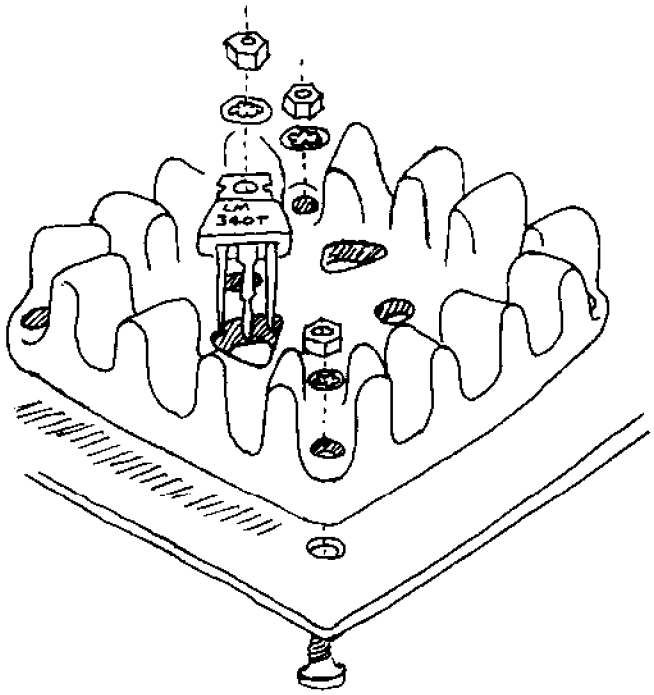


Figure 2-2. Heat sink and IC42 installation.

( ) Step 9. Install the two tantalum capacitors in the following locations. Take care to observe the proper value and orientation for each installation.

LOCATION	VALUE (ufd)	ORIENTATION
( ) C2	15	"+" lead top
( ) C3	1	"+" lead left

Check the capacitors for correct value and orientation, bend leads outward on solder (back) side of board, solder and trim.

( ) Step 10. Install all disc capacitors, except C25, in numerical order in the indicated locations. Insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of any wax. Reinsert and install.

Refer to footnote at the end of this step before installing asterisked (*) capacitors.

LOCATION	VALUE (ufd)	TYPE
( ) C1	.1	Disc Ceramic
( ) C4*	.1	Disc Ceramic
( ) C5*	.1	Disc Ceramic
( ) C6*	.1	Disc Ceramic
( ) C7	.1	Disc Ceramic
( ) C8	.1	Disc Ceramic
( ) C9*	.1	Disc Ceramic
( ) C10*	.1	Disc Ceramic
( ) C11*	.1	Disc Ceramic
( ) C12*	.1	Disc Ceramic
( ) C13*	.1	Disc Ceramic
( ) C14*	.1	Disc Ceramic
( ) C15*	.1	Disc Ceramic
( ) C16*	.1	Disc Ceramic
( ) C17*	.1	Disc Ceramic
( ) C18*	.1	Disc Ceramic
( ) C19*	.1	Disc Ceramic
( ) C20*	.1	Disc Ceramic
( ) C21*	.1	Disc Ceramic
( ) C22*	.1	Disc Ceramic
( ) C23*	.1	Disc Ceramic
( ) C24*	.1	Disc Ceramic
( ) C25	(Will be installed in Step 15.)	

*These capacitors must be positioned so that they fit between the IC's without touching them. To accomplish this, bend the leads as shown in Figure 2-3 on Page II-10 before inserting into board.

( ) Step 11. Install all resistors in numerical order in the indicated locations. Bend leads to fit distance between the mounting holes, insert, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim. Refer to footnote at the end of this step before installing asterisked (*) resistor.

(Step 11 continued on Page II-10.)

	LOCATION	VALUE (OHMS)	COLOR CODE
( )	R1	470	yellow-violet-brown
( )	R2	1.5K (or 2.2K)	brown-green-red**
( )	R3	470	yellow-violet-brown
( )	R4	1.5K (or 2.2K)	brown-green-red**
( )	R5	1.5K (or 2.2K)	" " " **
( )	R6	1.5K (or 2.2K)	" " " **
( )	R7	1.5K (or 2.2K)	" " " **
( )	R8	1.5K (or 2.2K)	" " " **
( )	R9	1.5K (or 2.2K)	" " " **
( )	R10	1.5K (or 2.2K)	" " " **
( )	R11	1.5K (or 2.2K)	" " " **
( )	R12	1.5K (or 2.2K)	" " " **
( )	R13*	39, 2 watt	orange-white-black
( )	R14	1.5K (or 2.2K)	brown-green-red**

*Do not install R13 unless you intend to use battery standby power.

**Red-red-red if 2.2K ohms.

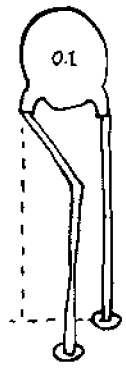


Figure 2-3. Disc capacitor lead formation for between IC's installation.

( ) Step 12. Install Augat pins as follows:

NOTE

You will find it helpful to hold the board between two objects so that it stands on one edge.

( ) Area A. Remove two pins from the carrier. Insert them into the mounting holes from front (component) side of board. Solder pins from back (solder) side of board so that the solder "wicks up" to the front side. (This will hold the pin firmly in place.)

Insert a component lead into one pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible. Repeat this procedure with the other pin.

NOTE

If the cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

Check both installations for cold joints and solder bridges.

( ) Area B. Remove three more pins from the carrier and install them in mounting holes P, C and U. Install these as you did the Area A pins. Check for cold joints and solder bridges.

( ) Area C. Remove the remaining three pins from the carrier and install them in mounting holes N, Y and W. Install these as you did the Area A pins. Check for cold joints and solder bridges.

( ) Area D. Augat pins are not supplied for this area since the 4KRA runs at maximum speed and requires no wait states. (Should you have three pins available and wish to install them in WF, 2 and 1, do so. Install them as you did the Area A pins and check for cold joints and solder bridges.)

( ) Step 13. Install DIP switch in its location below IC34. Position it so that the highest numbered switch is as far to the right as possible (the A12 mounting pads).

As you will note, the DIP switch mounting area will accommodate a 7-position switch. If a 7-position switch is supplied, only switches 4,5,6 and 7 are used for A15,A14,A13 and A12 respectively. With a 6-position switch, switches 3,4,5 and 6 are used, and with a 5-position switch, switches 2,3,4 and 5 are used. If a 4-position switch is supplied, switches 1,2, 3 and 4, of course, are used for A15,A14,A13 and A12 respectively.

( ) Step 14. Fill all exposed (not covered with lacquer) feed-through holes near the heat sink with solder.

( ) Step 15. Using the #24 bare wire, install jumpers in Areas A, B and C according to your selection of the options described in Section III.

( ) Step 16. Set DIP switches to select the desired starting address as described in Section III, Paragraph 3.5.

( ) Step 17. Check regulator operation. This check is made to prevent potential subsequent damage to the ICs from incorrect voltages.

( ) Install 4KRA in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON. TO DO SO CAN DAMAGE THE BOARD.

( ) Turn power on and measure the voltage between cathode of diode D3 (positive) and anode of diode D4 (ground). You should measure +5 V dc $\pm$5%.

( ) If voltage is incorrect, determine and correct the cause before proceeding. Especially check for solder shorts.

If voltage is correct, go on to Step 18.

( ) Step 18. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Pin 1 is positioned at the lower left corner of each IC location, and is indicated by a dot on the PC board and assembly drawing.

IC NO.		TYPE
( )	IC33	74LS05
( )	IC34	74LS136
( )	IC35	74LS00
( )	IC36	74LS13
( )	IC37	74367, 8097 or 8T97
( )	IC38	74367, 8097 or 8T97
( )	IC39	8836 or 8T380
( )	IC40*	74LS109 (not supplied)
( )	IC41	74LS132

*This IC, the "wait state counter" is not required since the 4KRA runs at maximum speed. IC40 is consequently not supplied with your kit. For special applications, a 74LS109 can be used in this location.

( ) Step 19. Install IC1 through IC32 in numerical order in their respective locations. Pay careful attention to the proper orientation.

NOTE

Pin 1 is indicated by a dot on the PC board and assembly drawing.

CAUTION

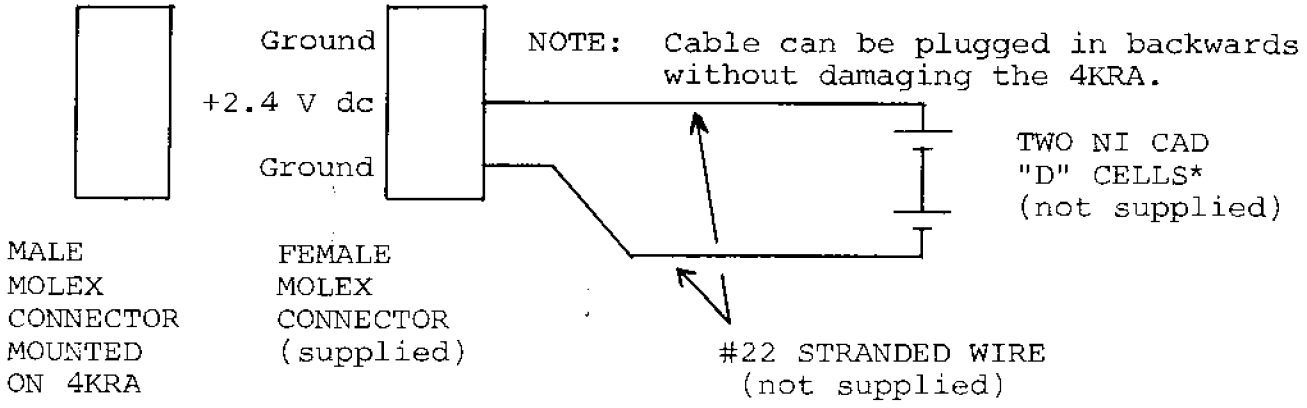
IC1 - IC32 (TYPE 91L02A or 21L02B) ARE MOS DEVICES. REFER TO CAUTION ON PAGE II-5.

( ) Step 20. Install the 4KRA in your computer and test it for proper operation. Test programs and instructions for testing the module are provided in Appendix V of this manual.

CAUTION

NEVER INSTALL OR REMOVE 4KRA WITH COMPUTER POWER ON.

( ) Step 21. If you intend to use the battery standby power feature of the 4KRA, fabricate a "cable" to interconnect the 4KRA and your standby supply. A mating connector for the male Molex you installed in Step 6 is provided for this purpose. Fabrication and power supply details are shown in Figure 2-4.



*Standard or alkaline batteries, with their attendant shorter life, may also be used. Recharging circuitry on the 4KRA continuously charges batteries during normal operation.

Figure 2-4. Standby power supply and interconnection.

SECTION III

OPTION SELECTION

4KRA STATIC READ/WRITE MEMORY MODULE

Processor Technology

3.1 OPTION SELECTION

Jumper options that control three operating parameters are provided on the 4KRA Memory Module. They are: phantom memory disable, power-up initialization and waiting time. The starting address for the module is selectable with four switches. Use the following selection instructions along with the assembly drawing in Section V.

3.2 MEMORY DISABLE OPTION (AREA A)

Select the phantom disable option only if the 4KRA is to be used at address zero with a Processor Technology ALS-8 Firmware Module. Selection is accomplished by installing a jumper (#24 bare wire is recommended) between the two Augat pins in Area A. With this jumper installed, the 4KRA will be disabled by the signal, PHANTOM, supplied by the ALS-8 on bus pin 67.

If the 4KRA is not to be used at address zero with the ALS-8, DO NOT install the Area A jumper.

3.3 POWER-UP INITIALIZATION OPTION (AREA B)

The jumper arrangement in Area B determines whether the 4KRA will come up in the protected or unprotected mode when power is initially applied or restored after a power failure. In the protect mode, a random operation cannot improperly rewrite retained data.

To select the power-up protect mode, install a jumper (#24 bare wire is recommended) between the C and P pins in Area B. On the solder (back) side of the board install C25 (.1 ufd disc ceramic capacitor) from GROUND to POINT U. (See Figure 3-1 on Page III-2.)

To select the power-up unprotect mode, install the jumper between the C and U pins in Area B. On the solder (back) side of the board install C25 (.1 ufd disc ceramic capacitor) from GROUND to POINT P. (See Figure 3-1 on Page III-2.)

3.4 WAITING TIME OPTIONS (AREAS C and D)

3.4.1 Wait State Enablement (Area C)

Since the 4KRA operates at maximum speed, you normally will not enable the wait state option.

To configure the 4KRA for no waiting time, install a jumper (#24 bare wire is recommended) between the W and N pins in Area C.

For special applications, you may wish to enable the wait state option. To do this, install a jumper between the W and Y pins in Area C.

(Paragraph 3.4.1 continued on Page III-2.)

NOTE

Enabling the wait state option has no meaning if IC40, the wait state counter, is not installed.

3.4.2 Number of Wait States (Area D)

The 4KRA can be configured for one or two wait states. Each wait state is 0.5 usec in duration.

To select one wait state, install a jumper (#24 bare wire is recommended) between the WF and 1 pins in Area D.

To select two wait states, install a jumper between WF and 2 pins in Area D.

NOTE

Wait states cannot be selected unless IC40, the wait state counter, and the W-to-Y jumper in Area C are installed.

3.5 STARTING ADDRESS SELECTION (DIP Switch)

One of 16 possible starting addresses for the 4KRA is selected by the settings of four switches (A15,A14,A13 and A12) in the DIP switch.

To select the desired address, set the A15, A14, A13 and A12 switches according to Table 3-1.

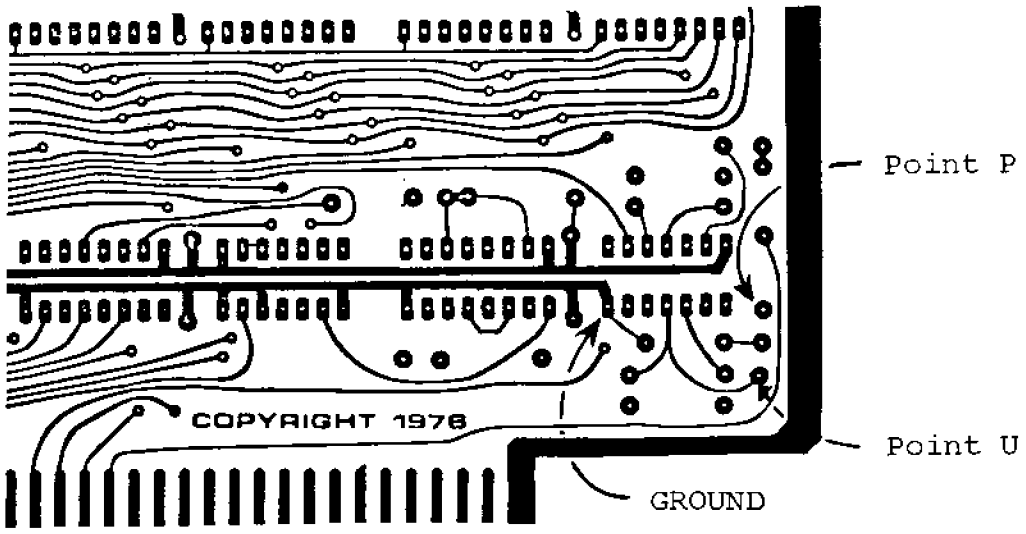


Figure 3-1. C25 installation for power-up initialization.

Table 3-1. 4KRA Starting Address Selection.

STARTING ADDRESS*		DIP SWITCH SETTINGS			
Decimal	Hex	A15	A14	A13	A12
0	0000	X	X	X	X
4,096	1000	X	X	X	C
8,192	2000	X	X	C	X
12,288	3000	X	X	C	C
16,384	4000	X	C	X	X
20,480	5000	X	C	X	C
24,576	6000	X	C	C	X
28,672	7000	X	C	C	C
32,768	8000	C	X	X	X
36,864	9000	C	X	X	C
40,960	A000	C	X	C	X
45,056	B000	C	X	C	C
49,152	C000	C	C	X	X
53,248	D000	C	C	X	C
57,344	E000	C	C	C	X
61,440	F000	C	C	C	C

X = switch open (OFF)
C = switch closed (ON)

*Only the indicated starting addresses are available. No intermediate addresses can be used.

SECTION IV

THEORY OF OPERATION

4KRA STATIC READ/WRITE MEMORY MODULE

Processor Technology

4.1 GENERAL DESCRIPTION

Refer to the 4KRA schematic diagram in Section V of this manual.

Address lines AØ through A9 are connected directly from the bus to the ten address input pins of each RAM (random access memory) chip, IC1 through IC32. The memory matrix consists of four, 8-bit word "pages". Only one page at a time, however, is selected to read information to, or write information from, the data buses.

In a memory write operation, the 4KRA writes data from the data-out bus, DOØ through DO7. Each data-out line is connected directly to the DI (data in) input of one RAM chip in each page of memory. Thus, each RAM chip in a page stores one bit of the word in that page.

In the memory read mode, the 4KRA reads information to the data-in bus, DIØ through DI7. The DO (data out) outputs of the RAMs are tri-state types that float in a high-impedance condition when they are not selected. They can therefore be--and are--connected in parallel from one page to the next. As a result, only the bits in the selected page can be gated to DIØ through DI7.

Full addressing of the 4KRA is done on AØ through A15, with each of the following segments performing the indicated function:

ADDRESS BITS	FUNCTION
AØ - A4	Selects row inside RAM chips (one of 32)
A5 - A9	Selects column inside RAM chips (one of 32)
AlØ - A11	Selects memory page (one of four)
A12 - A15	Selects 4KRA module (one of 16)

4.2 READ OPERATION

Data from the selected memory page is applied to tri-state bus drivers, IC37 and IC38. The drivers are enabled only if the output on pin 8 of IC36 is low, which only occurs when all four inputs are high.

Pin 8 of IC36 is low when: 1) SMEMR and PDBIN are high and SOUT and SINP are low, and 2) the wire OR'ed output of comparator IC34 (pins 3, 6, 8 and 11) is high. The first condition occurs when the processor requests, and is ready to receive, memory data. The second condition occurs when the address bits on A12 through A15 match the 4KRA address set-up by the jumpers (or DIP switch) in Area E. Thus the first condition exists for any memory read operation, but the second only occurs when the module is specifically addressed.

If the 4KRA is used at address zero with a Processor Technology ALS-8 Firmware Module, the Area A jumper will be in. Should this be the case, the 4KRA is disabled when the ALS-8 supplies a $\overline{\text{PHANTOM}}$ signal on bus pin 67.

Address bit A1Ø and A11 select the 1K memory page to be accessed. They are decoded in IC35 to supply a $\overline{\text{CE}}$Ø, $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ or $\overline{\text{CE3}}$ signal. The applicable signal enables the eight RAMs in the selected page.

In summary, A12 through A15 select the card, A1Ø and A11 select the memory page, and AØ through A9 select the word in the page to be read. The data is presented to the bus drivers, IC37 and IC38, which gate the data to the DI bus when the processor requests the data.

4.3 WRITE OPERATION

A write operation is similar to the read operation except MWRT is high instead of SMEMR. IC37 and 38 are disabled and pin 6 of IC36 is low for the duration of the MWRT pulse. The CPU controls the timing of this pulse. With pin 6 of IC36 low, all RAMs are partially enabled to read data from the DO bus. The page to be written into is selected by A1Ø and A11.

In order for pin 6 of IC36 to be low, pin 6 of IC41 must be high and the module must be selected (all outputs of IC34 are high). IC41 is connected as a latch which is set or reset by the PROT and UNPROT signals on bus pins 70 and 20. When PROT goes high to set the latch, pin 8 of IC41 goes high and pin 6 of IC41 goes low. This low inhibits $\overline{\text{WRITE ENABLE}}$ and provides an active low $\overline{\text{PS}}$ signal on pin 13 of IC38. A low $\overline{\text{PS}}$ turns computer PROT light on to indicate that the page of memory is protected. When UNPROT goes high, the latch resets so that pin 6 of IC41 is high to enable memory write operations on the card.

The jumper arrangement in Area B is used to select the power up protect or power up unprotect mode. In brief, Area B permits $\overline{\text{POC}}$ to perform the same function as PROT (C-to-P jumpered) or UNPROT (C-to-U jumpered) when computer power is turned on. If neither jumper is installed, it is necessary to issue the proper PROT or UNPROT signals to memory when first powering the computer to guarantee a known state.

4.4 WAIT STATES

The RAM chips supplied with the 4KRA provide valid data within one CPU cycle time (500 nanoseconds). When such fast RAMs are used, the Area C jumper which selects waiting time is connected to the N terminal, which connects a "high" level to pin 12 of IC38. When this section of the bus driver is enabled (low on pin 15) by a low on pin 3 of IC39, the PRDY signal to the bus is driven high.

Therefore, the memory card sends a "ready" signal back as soon as it is addressed. The data will be ready before the processor is.

In certain special applications, or if slower RAM chips or a faster CPU are used, one or two "wait" cycles must be allowed to pass before the CPU is allowed to accept the data. IC40 comprises a two-bit shift register which may be selected to give a high level at pin 6 after one or two PSYNC pulses. IC40 is a dual J-K flip-flop with positive clock. The outputs of each section change on the low-to-high transition of the clock signal, depending on the condition of the J and $\overline{K}$ inputs. The changes occur according to the following table:

J low, $\overline{K}$ high ..... no change
J high, $\overline{K}$ high ..... Q goes high
J low, $\overline{K}$ low ..... Q goes low
J high, $\overline{K}$ low .... Q changes to the opposite level

When PSYNC goes high section 2 is reset, if it was not already reset. Pin 6 goes low and since both J and $\overline{K}$ inputs to section 1 are now low, section 1 Q goes low on the high-to-low transition of Ø2 clock.

When PSYNC goes low, section 2 may change state on the next high-to-low Ø2 transition. If the J input (pin 2) is high, section 2 will be set on the next high-to-low transition of Ø2. This will happen if the jumper is connected from W to 1. The same clock transition will cause section 1 to change state. Note that the "old" data at the output of section 2 is what counts for this clock transition. The "new" data does not appear at the outputs until some time after the clock transition.

Now both sections are set. Since pin 2 is now low and pin 3 high, section 2 will remain this way until PSYNC resets it. The same conditions hold true at the inputs to section 1, so it will remain without changing state.

If the jumper was connected to 2 (pin 10), then section 2 would not set on the first clock pulse after PSYNC. Section 1 would still change state on this transition, however. The conditions would then be correct to allow section 2 to set on the next clock pulse. Section 1 would change state again on that transition. The two sections would then "lock up" with section 1 reset and section 2 set.

Thus, if IC40 is installed and the wait states are jumpered in, pin 6 will go high on the first high-to-low transition of Ø2 after PSYNC if 1 wait state is selected. Pin 6 will go high on the second high-to-low transition of Ø2 after PSYNC if 2 wait states have been selected. Pin 6 will in either case remain high until the next PSYNC.

4.5 POWER SUPPLY

IC42, a series voltage regulator, supplies on-card regulation, maintaining a constant 5 V dc output. Input bypass capacitor (C3) provides additional filtering of the 8 V dc input, and the output bypass capacitor (C2) improves transient response by attenuating transients.

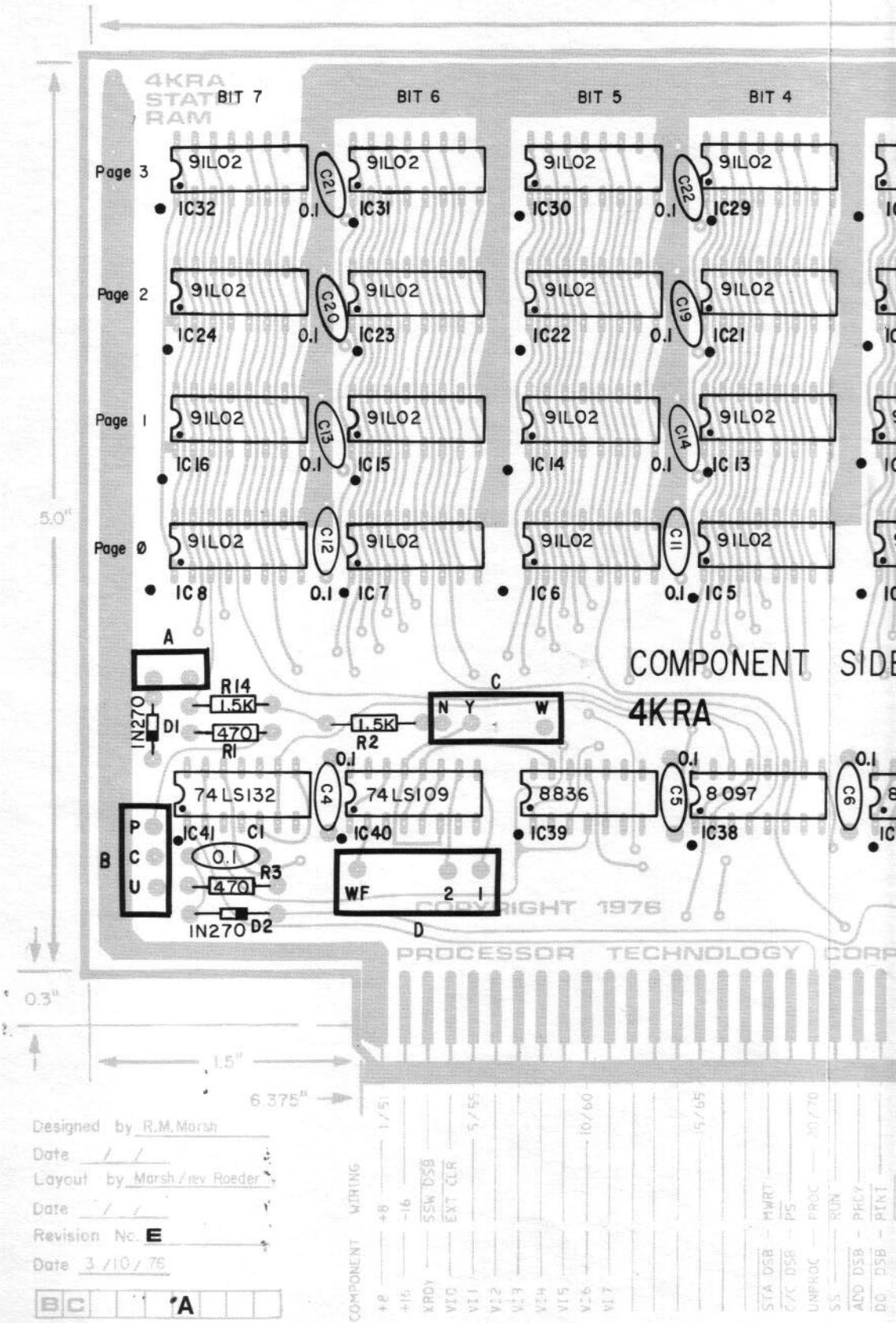
Diode D4 is a protective shunt that prevents damage to the 4KRA if it is plugged into the computer backwards. D5 and limiting resistor R13 permit the standby battery supply, if used, to continuously charge during normal operation. Should there be a power loss, and the standby power supply is connected, D3 conducts to make battery power available to the 4KRA. Under normal operating conditions, D3 isolates the standby supply from +5 V dc.

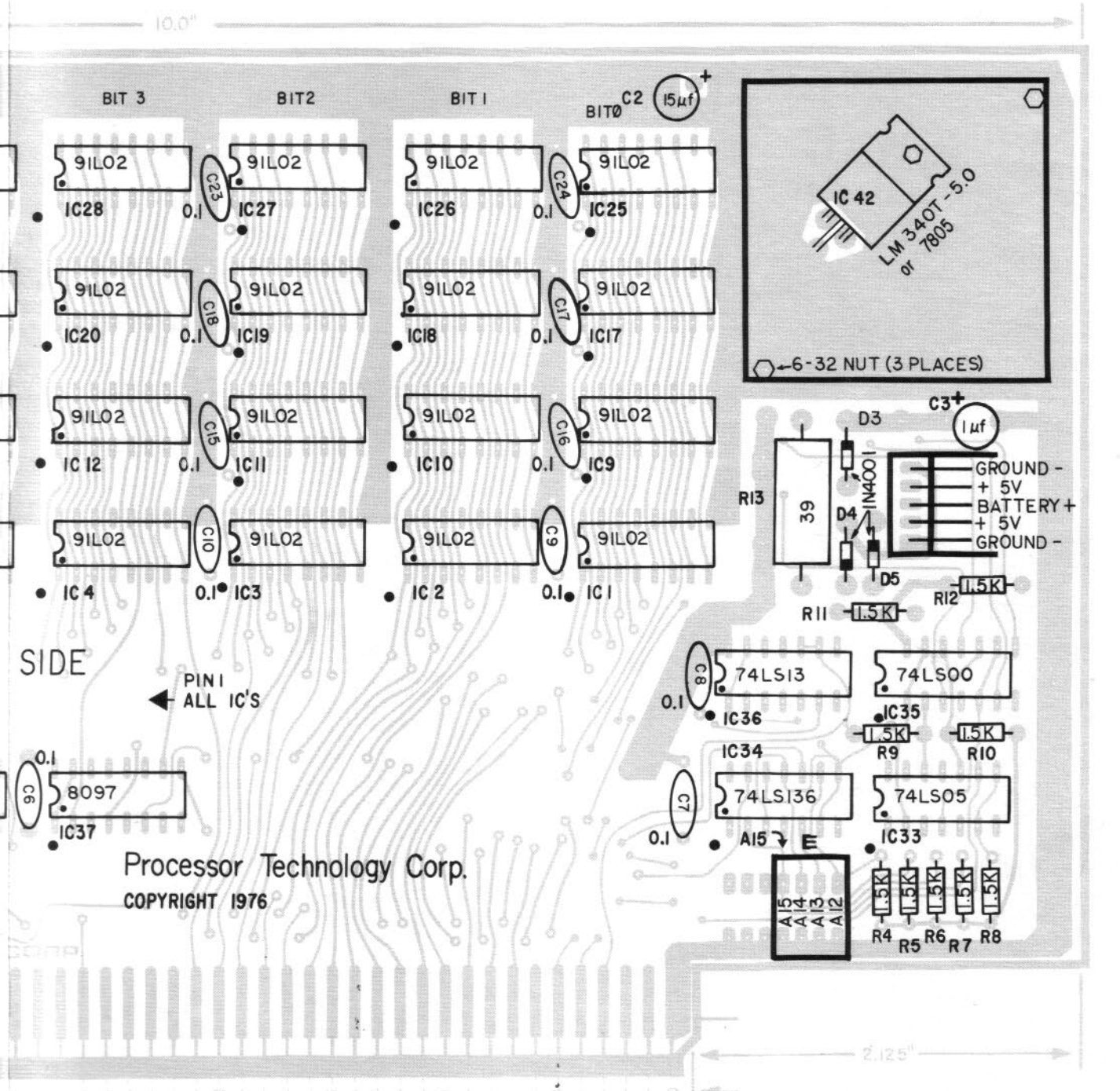
SECTION V

DRAWINGS

4KRA STATIC READ/WRITE MEMORY MODULE

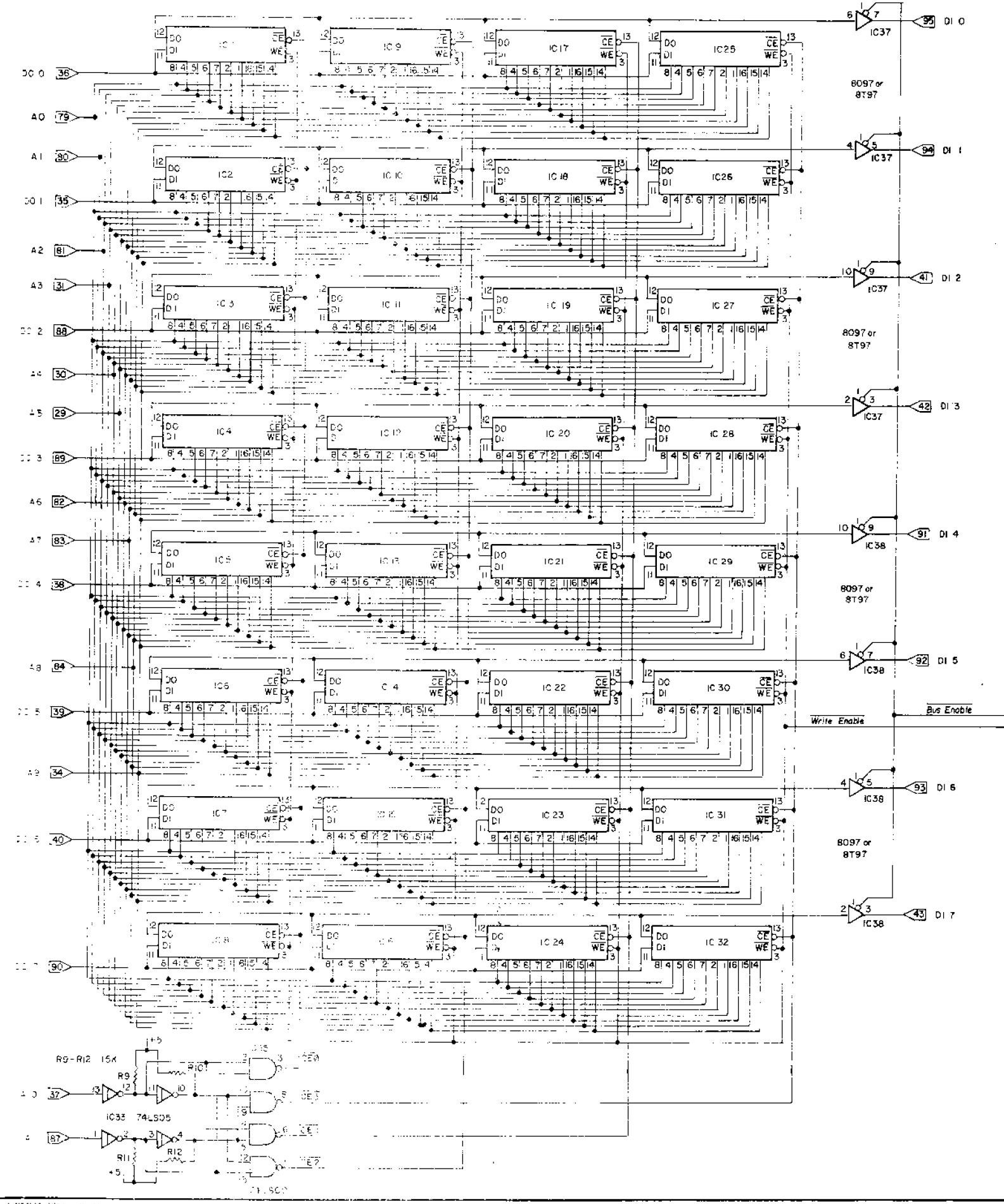
Processor Technology

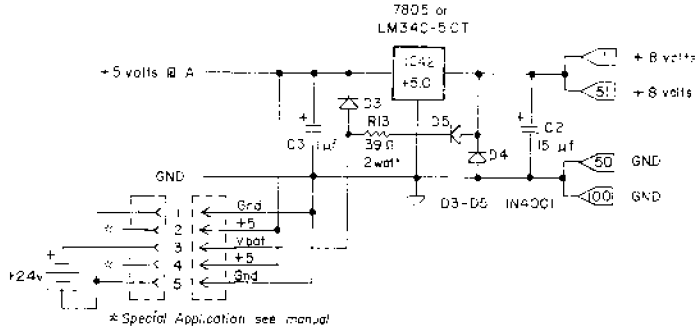

4KRA
STAT
RAM
BIT 7
BIT 6
BIT 5
BIT 4
Page 3
Page 2
Page 1
Page Ø
91LO2
IC32
IC31
IC30
IC29
IC24
IC23
IC22
IC21
IC16
IC15
IC14
IC13
IC8
IC7
IC6
IC5
C21
C22
C20
C19
C13
C14
C12
C11
0.1
5.0"
A
R14
1.5K
470
R1
IN270
D1
1.5K
R2
C
N Y W
COMPONENT SIDE
4KRA
74LS132
74LS109
8836
8097
IC41
IC40
IC39
IC38
C4
C5
C6
C1
0.1
R3
470
IN270
D2
B
P
C
U
WF 2 1
D
COPYRIGHT 1976
PROCESSOR TECHNOLOGY CORP
0.3"
1.5"
6.375"
Designed by R.M.Marsh
Date / /
Layout by Marsh / rev. Roeder
Date / /
Revision No. E
Date 3/10/76
B C A



Processor Technology Co.
Standard Card Layout

Title 4K RA ASSEMBLY


DO 0
A0
A1
DO 1
A2
A3
DO 2
A4
A5
DO 3
A6
A7
DO 4
A8
DO 5
A9
DO 6
DO 7
A10
A11
A12
DI 0
DI 1
DI 2
DI 3
DI 4
DI 5
DI 6
DI 7
8097 or 8T97
IC37
IC38
Write Enable
Bus Enable
R9-R12 15K
IC33 74LS05



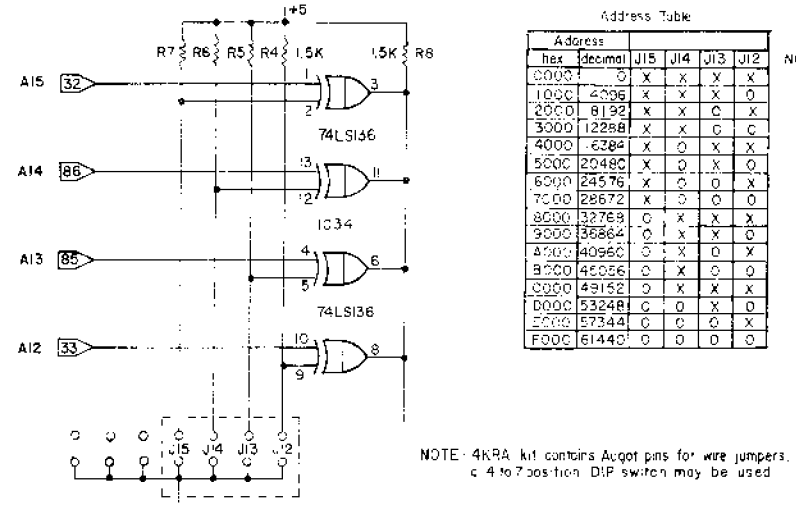
Address Table

Address					
hex	decimal	JI5	JI4	JI3	JI2
0000	0	X	X	X	X
1000	4096	X	X	X	0
2000	8192	X	X	0	X
3000	12288	X	X	0	0
4000	16384	X	0	X	X
5000	20480	X	0	X	0
6000	24576	X	0	0	X
7000	28672	X	0	0	0
8000	32768	0	X	X	X
9000	36864	0	X	X	0
A000	40960	0	X	0	X
B000	45056	0	X	0	0
C000	49152	0	0	X	X
D000	53248	0	0	X	0
E000	57344	0	0	0	X
F000	61440	0	0	0	0

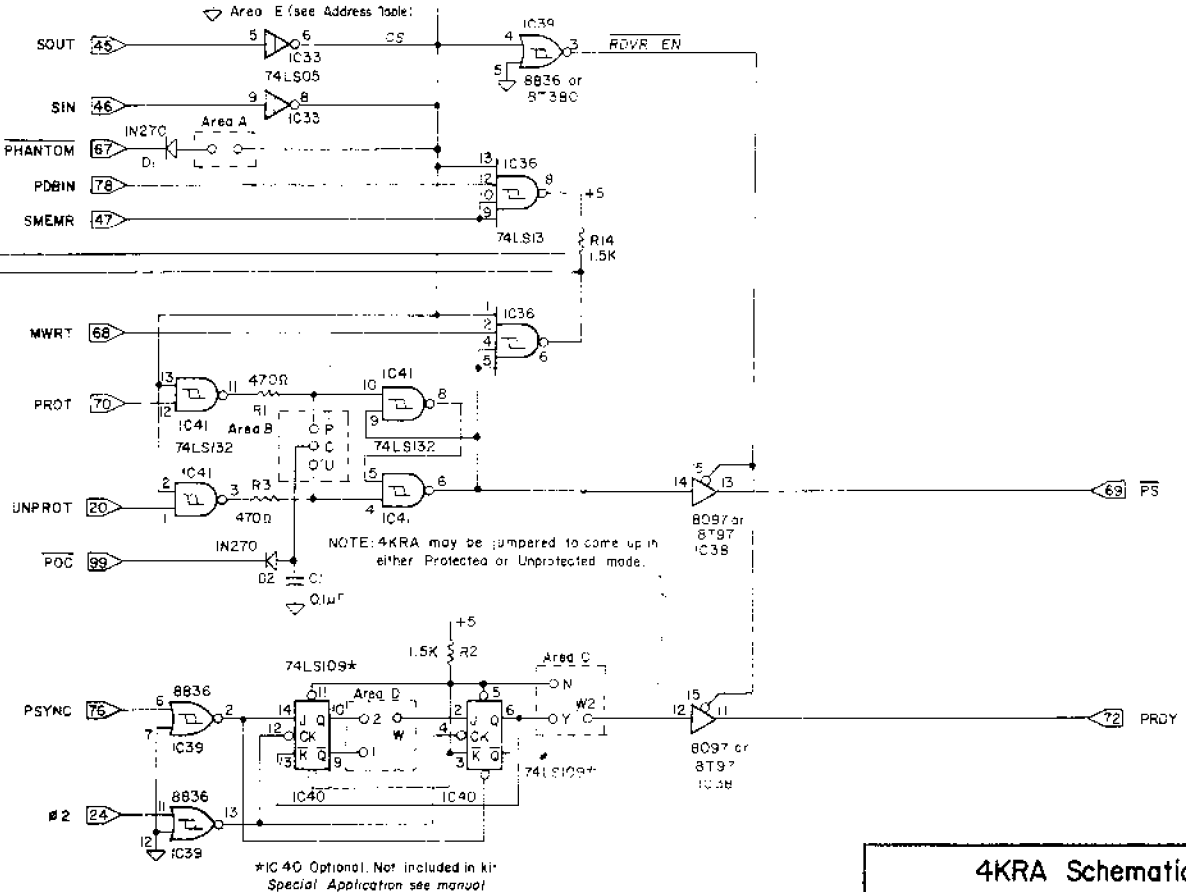
NOTE: "X" indicate jumpers installed or switch on
"O" indicate no jumper installed or switch off

NOTE: 1) All resistors 1/4 watt unless otherwise stated

2) IC1 through IC25 are 91L02 static 1024 x 1 bit RAM's. All RAM are either 91L02A or electrically equivalent versions



NOTE: 4KRA kit contains Augat pins for wire jumpers. a 4 to 7 position DIP switch may be used



4KRA Schematic

SCALE 806C	Designed by:	DRAWN BY Roeder
DATE 3/76	Robert M. Marsh	REVISED 3/76

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4096 x 8 bit low power static RAM board
Designed to be used by 8080 processors

Board Rev (0)
Dwg Rev (0)

APPENDICES

4KRA STATIC READ/WRITE MEMORY MODULE

Processor Technology

Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit directly from **Processor Technology** and returned to the factory within the three-month warranty period, which in the judgement of **PTC** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, without charge. Kits purchased from authorized **PTC** dealers should be returned to the selling dealer for the same warranty service.

Any modules purchased as a kit and returned to **PTC,** which in the judgement of **PTC** are not covered by the above conditions, will be repaired and returned at a cost commensurate with the work required. In any case, this charge will not exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

00	NOP		28	-		50	MOV	D,B	78	MOV	A,B	A0	ANA	B	C8	RZ		F0	RP				
01	LXI	B D16	29	DAD	H	51	MOV	D,C	79	MOV	A,C	A1	ANA	C	C9	RET		F1	POP	PSW			
02	STAX	B	2A	LHLD	Adr	52	MOV	D,D	7A	MOV	A,D	A2	ANA	D	CA	JZ		F2	JP	Adr			
03	INX	B	2B	DCX	H	53	MOV	D,E	7B	MOV	A,E	A3	ANA	E	CB	- - -		F3	DI				
04	INR	B	2C	INR	L	54	MOV	D,H	7C	MOV	A,H	A4	ANA	H	CC	CZ	Adr	F4	CP	Adr			
05	DCR	B	2D	DCR	L	55	MOV	D,L	7D	MOV	A,L	A5	ANA	L	CD	CALL	Adr	F5	PUSH	PSW			
06	MVI	B D8	2E	MVI	L,D8	56	MOV	D,M	7E	MOV	A,M	A6	ANA	M	CE	ACI	D8	F6	ORI	D8			
07	RLC		2F	CMA		57	MOV	D,A	7F	MOV	A,A	A7	ANA	A	CF	RST	1	F7	RST	6			
08	- - -		30	- - -		58	MOV	E,B	80	ADD	B	A8	XRA	B	D0	RNC		F8	RM				
09	DAD	B	31	LXI	SP,D16	59	MOV	E,C	81	ADD	C	A9	XRA	C	D1	POP	D	F9	SPHL				
0A	LDAX	B	32	STA	Adr	5A	MOV	E,D	82	ADD	D	AA	XRA	D	D2	JNC	Adr	FA	JM	Adr			
0B	DCX	B	33	INX	SP	5B	MOV	E,E	83	ADD	E	AB	XRA	E	D3	OUT	D8	FB	EI				
0C	INR	C	34	INR	M	5C	MOV	E,H	84	ADD	H	AC	XRA	H	D4	CNC	Adr	FC	CM	Adr			
0D	DCR	C	35	DCR	M	5D	MOV	E,L	85	ADD	L	AD	XRA	L	D5	PUSH	D	FD	- - -				
0E	MVI	C D8	36	MVI	M,D8	5E	MOV	E,M	86	ADD	M	AE	XRA	M	D6	SUI	D8	FE	CPI	D8			
0F	RRC		37	STC		5F	MOV	E,A	87	ADD	A	AF	XRA	A	D7	RST	2	FF	RST	7			
10	- - -		38			60	MOV	H,B	88	ADC	B	B0	ORA	B	D8	RC							
11	LXI	D D16	39	DAD	SP	61	MOV	H,C	89	ADC	C	B1	ORA	C	D9	- - -							
12	STAX	D	3A	LDA	Adr	62	MOV	H,D	8A	ADC	D	B2	ORA	D	DA	JC	Adr						
13	INX	D	3B	DCX	SP	63	MOV	H,E	8B	ADC	E	B3	ORA	E	DB	IN	D8						
14	INR	D	3C	INR	A	64	MOV	H,H	8C	ADC	H	B4	ORA	H	DC	CC	Adr						
15	DCR	D	3D	DCR	A	65	MOV	H,L	8D	ADC	L	B5	ORA	L	DD	- - -							
16	MVI	D,D8	3E	MVI	A,D8	66	MOV	H,M	8E	ADC	M	B6	ORA	M	DE	SBI	D8						
17	RAL		3F	CMC		67	MOV	H,A	8F	ADC	A	B7	ORA	A	DF	RST	3						
18	- - -		40	MOV	B,B	68	MOV	L,B	90	SUB	B	B8	CMP	B	E0	RPO							
19	DAD	D	41	MOV	B,C	69	MOV	L,C	91	SUB	C	B9	CMP	C	E1	POP	H						
1A	LDAX	D	42	MOV	B,D	6A	MOV	L,D	92	SUB	D	BA	CMP	D	E2	JPO	Adr						
1B	DCX	D	43	MOV	B,E	6B	MOV	L,E	93	SUB	E	BB	CMP	E	E3	XTHL							
1C	INR	E	44	MOV	B,H	6C	MOV	L,H	94	SUB	H	BC	CMP	H	E4	CPO	Adr						
1D	DCR	E	45	MOV	B,L	6D	MOV	L,L	95	SUB	L	BD	CMP	L	E5	PUSH	H						
1E	MVI	E,D8	46	MOV	B,M	6E	MOV	L,M	96	SUB	M	BE	CMP	M	E6	ANI	D8						
1F	RAR		47	MOV	B,A	6F	MOV	L,A	97	SUB	A	BF	CMP	A	E7	RST	4						
20	- - -		48	MOV	C,B	70	MOV	M,B	98	SBB	B	C0	RNZ		E8	RPE							
21	LXI	H D16	49	MOV	C,C	71	MOV	M,C	99	SBB	C	C1	POP	B	E9	PCHL							
22	SHLD	Adr	4A	MOV	C,D	72	MOV	M,D	9A	SBB	D	C2	JNZ	Adr	EA	JPE	Adr						
23	INX	H	4B	MOV	C,E	73	MOV	M,E	9B	SBB	E	C3	JMP	Adr	EB	XCHG							
24	INR	H	4C	MOV	C,H	74	MOV	M,H	9C	SBB	H	C4	CNZ	Adr	EC	CPE	Adr						
25	DCR	H	4D	MOV	C,L	75	MOV	M,L	9D	SBB	L	C5	PUSH	B	ED	- - -							
26	MVI	H D8	4E	MOV	C,M	76	HLT		9E	SBB	M	C6	ADI	D8	EE	XRI	D8						
27	DAA		4F	MOV	C,A	77	MOV	M,A	9F	SBB	A	C7	RST	0	EF	RST	5						

HEX-ASCII TABLE

Printing		Characters	
30	0	40	@
31	1	20	space
32	2	21	!
33	3	22	"
34	4	23	#
35	5	24	$
36	6	25	%
37	7	26	&
38	8	27	'
39	9	28	(
		29	)
41	A	2A	*
42	B	2B	+
43	C	2C	,
44	D	2D	-
45	E	2E	.
46	F	2F	/
47	G	3A	:
48	H	3B	;
49	I	3C	<
4A	J	3D	=
4B	K	3E	>
4C	L	3F	?
4D	M	5B	[
4E	N	5C	\
4F	O	5D	]
50	P	5E	↑ (^)
51	Q	5F	← (_)
52	R		
53	S		
54	T		
55	U		
56	V		
57	W		
58	X		
59	Y		
5A	Z		

HEX-ASCII TABLE

Non-Printing

00	NULL
07	BELL
09	TAB
0A	LF
0B	VT
0C	FORM
0D	CR
11	X-ON
12	TAPE
13	X-OFF
14	
1B	ESC
7D	ALT MODE
7F	RUB OUT

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

Processor Technology Corp.

APPENDIX II

JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L

77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

CONSTANT DEFINITION

0BDH, 1AH	Hex
105D, 105	Decimal
720, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A', 'B'	ASCII

OPERATORS

MOVE IMMEDIATE

06	MVI	B,	D8
0E	MVI	C,	
16	MVI	D,	
1E	MVI	E,	
26	MVI	H,	
2E	MVI	L,	
36	MVI	M,	
3E	MVI	A,	

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	
D6	SUI	
DE	SBI	
E6	ANI	
EE	XRI	
F6	ORI	
FE	CPI	

LOAD IMMEDIATE

01	LXI	B,	D16
11	LXI	D,	
21	LXI	H,	
31	LXI	SP,	

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[,]
DW	D16	[,]

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

* = all Flags (C,Z,S,P) affected

† = only CARRY affected

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron — 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

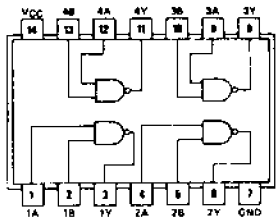
(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

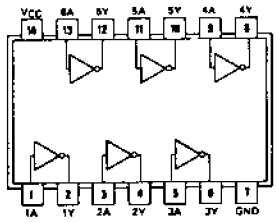
(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

7400 or 74LS00



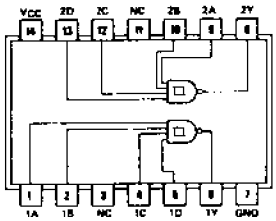
positive logic:
$Y = \overline{AB}$

74LS05



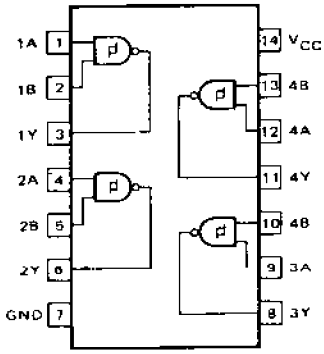
positive logic:
$Y = \overline{A}$

74LS13



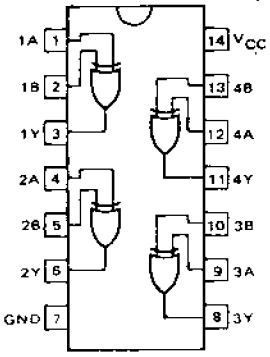
positive logic:
$Y = \overline{ABCD}$

74LS132



positive logic: $Y = \overline{AB}$

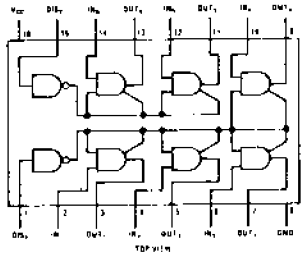
74LS136



INPUTS		OUTPUT
A	B	y
L	L	L
L	H	H
H	L	H
H	H	L

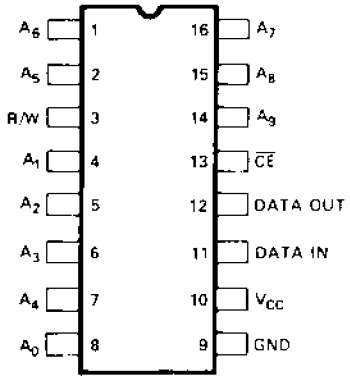
H = high level, L = low level

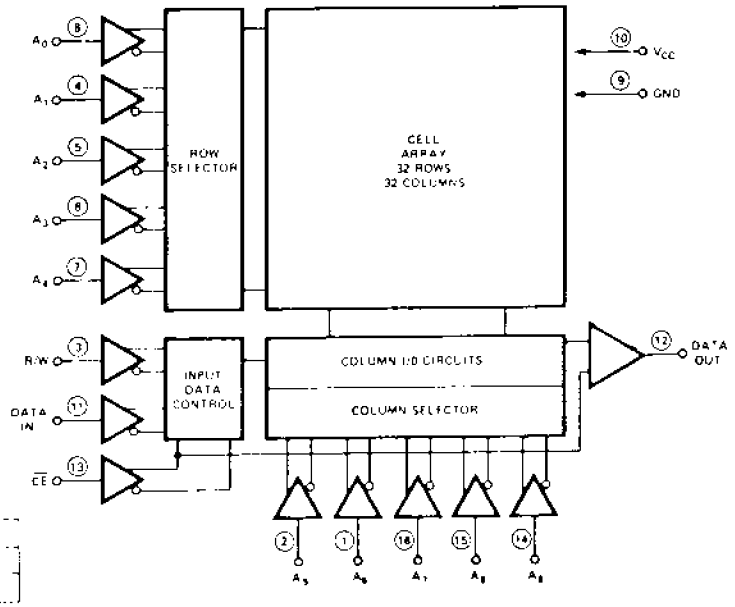
74367, 8097 or 8T97



DISABLE DIS_A	INPUT DIS_Z	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	Hz*
1	X	X	Hz**

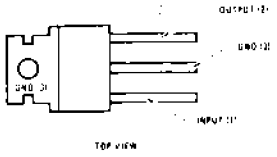
91L02A or 21L02B

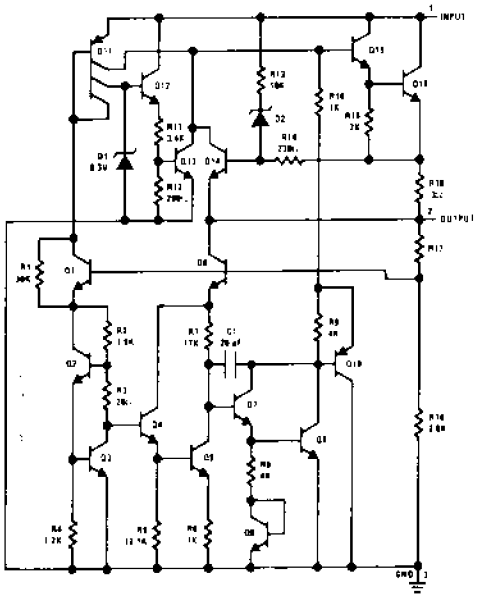




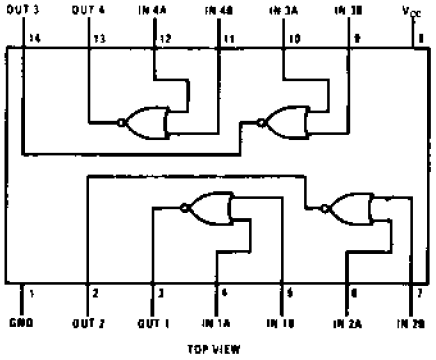
D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
A_0-A_9	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

340T-5.0 or 7805UC





8836 or 8T380



V.1 4K MEMORY TEST

The 4K memory test will effectively test any 4K segment of memory. The incrementing pattern used for the test will find errors in any but the most cantankerous, pattern sensitive, dynamic memory.

The test is performed in two segments: write and read. Write begins at the bottom of the 4K address (LOAD), writing zero and then writing an incrementing pattern to the "top". After each location is read and compared to its proper pattern, and if no errors are found, the starting pattern is incremented and the test is once again performed.

This read-write sequence continues until an error is found or until the machine is halted. If an error is found, all information relating to the error is saved in locations ØØØ - ØØ6.

ADDRESS	
5	High Address Error Pointer
4	Low Address Error Pointer
3	Write Data
2	Read Data (Error)
1	Page Down Count

V.1.1 Test Procedure

To use the test program given in Paragraph V.1.2, proceed as follows:

( ) Step 1. Clear memory locations ØØØØ through ØØØ6 and load the hex code starting from location ØØØ7.

( ) Step 2. As the code is entered, check the address for each input as a test of proper code and location.

( ) Step 3. Check each location for the proper bits after all code is entered.

( ) Step 4. Press RESET and RUN switches. The test should proceed as indicated by the address lights.

NOTE

A full test of all 256 bit patterns to all 4096 locations takes about 30 seconds with a fast memory.

( ) Step 5. Repeat test for one hour with the computer cover in place.

V.1.2 4K Memory Test Program

```
0000                          0000 *    <<< 4K MEMORY TEST PROGRAM    >>>
0000                          0001 *
0000                          0002 *  ASSEMBLED ON SOFTWARE PACKAGE #1
0000                          0008 LOAD EQU 4096
0000                          0009 TOP EQU 32
0000                          0010 SP EQU 6
0000                          0015 *
0000                          0020  ORG 7
0007                          0025 *
0007 31 06 00                 0030 START   LXI  SP, 6  SET UP ERROR CATCH
000A AF                       0035         XRA  A      CLEAR REG A
000B 47                       0040         MOV  B,A    CLEAR B
000C                          0045 *
000C 21 00 10                 0050 OVER    LXI  H, LOAD  LOAD ADDRESS
000F 48                       0053         MOV  C,B    FIRST WRITE DATA
0010 71                       0055 WRITE   MOV  M,C    PUT IN MEMORY
0011 23                       0060         INX  H      NEXT ADDR
0012 0C                       0065         INR  C      NEXT WRITE DATA
0013 7C                       0070         MOV  A,H
0014 FE 20                    0075         CPI  TOP    IS H OVER THE TOP?
0016 C2 10 00                 0080         JNZ  WRITE  IF NOT THEN MORE
0019                          0081 *
0019                          0082 *   READ TEST ROUTINE
0019                          0083 *
0019 78                       0085         MOV  A,B    GET FIRST WRITE DATA
001A 0E 04                    0090         MVI  C,4    C HOLDS PAGE COUNT
001C 21 00 10                 0095         LXI  H, LOAD  LOAD ADDRESS
001F                          0096 *
001F 11 00 04                 0100 NEXT    LXI  D, 1024  D-E COUNT K'S
0022 BE                       0110 READ    CMP  M        IS DATA OK?
0023 C2 3B 00                 0112         JNZ  ERROR IF NOT CATCH IT
0026 1D                       0115         DCR  E
0027 C2 2E 00                 0118         JNZ  OKTES
002A 15                       0120         DCR  D     ANOTHER PAGE DOWN
002B CA 33 00                 0125         JZ   ONEK  COUNT K'S
002E                          0133 *
002E 23                       0135 OKTES   INX  H     NEXT ADDRESS
002F 3C                       0140         INR  A
0030 C3 22 00                 0145         JMP  READ
0033                          0146 *
0033 0D                       0150 ONEK    DCR  C     ONE MORE K DOWN
0034 C2 1F 00                 0155         JNZ  NEXT  MORE K'S TO COUNT
0037 04                       0157         INR   B
0038 C3 0C 00                 0160         JMP  OVER
003B                          0170 *
003B                          0175 *     ERROR STUFF ROUTINE
003B                          0180 *
003B                          0185 *  ADDRESS
003B                          0186 *    5  HAS HIGH ERROR ADDR
003B                          0187 *    4  HAS LOW   "   "
```

```
003B                    0188 *    3  HAS WRITE DATA
003B                    0189 *    2  HAS READ DATA (ERROR)
003B                    0190 *    0  HAS PAGE DOWN COUNT
003B                    0210 *
003B                    0215 *
003B E5                 0216 ERROR    PUSH  H    STUFF ADDRESSES
003C 57                 0220          MOV   D,A  GET WRITE DATA
003D 5E                 0225          MOV   E,M  GET READ DATA
003E D5                 0230          PUSH  D    PUT ON STACK
003F C5                 0235          PUSH  B    ALL OF IT
0040 76                 0240 AHHHH    HLT      STOP THIS NONSENSE
0041                    0245 *
0041                    0250 *
```

V.2 4KRA MEMORY TEST

The 4KRA memory test is designed to detect faulty memory bits and identify the general area in which a malfunction exists. To use this test, you will need a printer with an ESCAPE function.

V.2.1 Test Procedure

To use the test program given in Paragraph V.2.2, proceed as follows:

NOTE 1

The 4KRA to be tested must be in the unprotected power-up initialization mode (see Paragraph 3.3 in Section III of this manual).

NOTE 2

A 4KRA used to store the test program cannot be selected for testing.

( ) Step 1. Load test program into memory starting at location ØØØØ.

( ) Step 2. Set starting address of the 4KRA to be tested into Sense Switches 12 through 15. (These Sense Switches are set to the four highest order bits--A15, A14, A13 and A12--recognized by the module under test.) For example, set Switch 15 on (1) and Switches 14 through 12 off (Ø) to test a 4KRA with a starting address of 8ØØØ (Hex).

( ) Step 3. Start test by pressing RESET and RUN switches in that order.

NOTE

The test takes a minute or so to run. When it is done, a print routine will print a map that corresponds to the IC memory layout on the 4KRA board; that is, four eight-bit rows.

( ) Step 4. Analyze the map to determine which bits are defective. An example follows:

```
BIT NO.  7 6 5 4 3 2 1 0 ←(IC25)
(IC32)→  X G G G G G G G  Page 3
         G G G G G G G G  Page 2
         G G G G G G G G  Page 1
(IC8) →  X G G G G G G G  Page 0
                    (IC1)
```

A "G" indicates all bits in the corresponding IC memory (IC25 for example) are good. An "X" indicates that one or more of the bits in the corresponding IC memory (IC28 for example) are defective. A defective bit, or bits, can be caused by a bad IC memory or a defect in one or more of the decoding and interface ICs.

( ) Step 5. The test may be repeated by striking the ESCAPE key.

NOTE

To test another 4KRA, set new address into Sense Siwtches and strike ESCAPE key.

V.2.2 4KRA Memory Test Program

```
0000                    1040 * ASSEMBLED ON THE  ALS-8 SOFTWARE
0000                    1045 * DEVELOPMENT SYSTEM
0000                    1050 *
0000 F3                 1055        DI          DISABLE INTERUPTS
0001 DB 01              1060        IN    KBDI  CLEAR KEYBOARD READY
0003 31 AA 01           1065 BGIN   LXI   SP,AREA+20H /RESTARTING POINT
0006 CD 38 00           1070        CALL  CRLF  RESTART FROM ESC
0009 DB FF              1075 INSS   IN    0FFH  READ SENSE SWITCHES
000B E6 F0              1080        ANI   0F0H  MASK LOWER FOUR
000D CA 09 00           1085        JZ    INSS  NOT ALLOWED
0010 67                 1090        MOV   H,A   SET UP START ADDRESS
0011 2E 00              1095        MVI   L,0
0013 22 5A 01           1100        SHLD  BBUF  STORE START ADDRESS
0016 21 00 00           1105        LXI   H,0   /CLEAR MAP
0019 22 52 01           1110        SHLD  EBUF
001C 22 54 01           1115        SHLD  EBUF+2
001F                    1120 *  END = START + 4K
001F 2A 5A 01           1125        LHLD  BBUF
0022 3E 10              1130        MVI   A, 10H
0024 84                 1135        ADD   H
0025 67                 1140        MOV   H,A
0026 2B                 1145        DCX   H
0027 22 5C 01           1150        SHLD  BBUF+2 /STORE END ADRS
002A C3 62 00           1155        JMP   MRCK  GO TO MEMORY CHECK
002D                    1160 *
002D DB 00              1165 OUT8   IN    VIDS  READ I/O STATUS
002F E6 80              1170        ANI   80H
0031 CA 2D 00           1175        JZ    OUT8  WAIT
0034 78                 1180        MOV   A,B
0035 D3 01              1185        OUT   VIDO  XMIT DATA
0037 C9                 1190        RET
0038                    1195 *
0038 06 0D              1200 CRLF   MVI   B,13  WRITE CR LF & 2 RUBOUTS
003A CD 2D 00           1205        CALL  OUT8
003D 06 0A              1210        MVI   B,10
003F CD 2D 00           1215        CALL  OUT8
0042 06 7F              1220        MVI   B,127
```

```
0044 CD 2D 00          1225          CALL  OUT8
0047 CD 2D 00          1230          CALL  OUT8
004A C9                1235          RET
004B                   1240 *
004B 2A 5A 01          1245 ACHK     LHLD  BBUF     FETCH ADDRESS
004E 3A 5D 01          1250          LDA   BBUF+3   STOP ADDRESS
0051 BC                1255          CMP   H        COMPARE HIGH ADDRESS
0052 C2 5D 00          1260          JNZ   ACH1
0055 3A 5C 01          1265          LDA   BBUF+2   STOP ADDRESS LOW
0058 BD                1270          CMP   L
0059 C2 5D 00          1275          JNZ   ACH1
005C 37                1280          STC            SET CARRY IF EQUAL
005D                   1285 *
005D 23                1290 ACH1     INX   H        INCREMENT START ADDRESS
005E 22 5A 01          1295          SHLD  BBUF     STORE INCR START ADDRESS
0061 C9                1300          RET
0062                   1305 *
0062 21 01 00          1310 MRCK     LXI   H,1      INITIALIZE PASS COUNT
0065 22 6E 01          1315          SHLD  DBUF+4   STORE IT
0068 2A 5A 01          1320 MRC1     LHLD  BBUF     GET START LOCATION
006B E5                1325          PUSH  H        SAVE START LOCATION
006C AF                1330          XRA   A        INITIALIZE MASTER PATTERN
006D 37                1335          STC            SET CARRY
006E F5                1340          PUSH  PSW      STORE MASTER PATTERN
006F                   1345 *
006F F5                1350 WRL1     PUSH  PSW      SAVE WORKING PATTERN
0070 77                1355          MOV   M,A      PATTERN 1 TO MEMORY
0071 CD 4B 00          1360          CALL  ACHK     CHECK IF LAST, INCREMENT
0074 DA 7C 00          1365          JC    RDL1     DONE WRITING PATTERN
0077 F1                1370          POP   PSW      GET WORKING PATTERN
0078 17                1375          RAL            SHIFT WORKING PATTERN
0079 C3 6F 00          1380          JMP   WRL1     DO MORE WRITING
007C                   1385 *
007C F1                1390 RDL1     POP   PSW      UNLOAD STACK
007D F1                1395          POP   PSW      GET MASTER PATTERN
007E E1                1400          POP   H        RESTORE START LOCATION
007F 22 5A 01          1405          SHLD  BBUF     STORE START
0082 E5                1410          PUSH  H        SAVE START
0083 F5                1415          PUSH  PSW      SAVE MASTER PATTERN
0084                   1420 *
0084 F5                1425 RDL2     PUSH  PSW      SAVE WORKING PATTERN
0085 BE                1430          CMP   M        CHECK IT
0086 C4 F4 00          1435          CNZ   MTER     READ ERROR
0089 CD E5 00          1440          CALL  ESCP     CHECK FOR ESCAPE
008C CD 4B 00          1445          CALL  ACHK     SEQUENCE LOCATION
008F DA 97 00          1450          JC    NXP1     NEXT PATTERN 1
0092 F1                1455          POP   PSW      GET WORKING PATTERN
0093 17                1460          RAL            SHIFT WORKING PATTERN
0094 C3 84 00          1465          JMP   RDL2     DO MORE
0097                   1470 *
0097 F1                1475 NXP1     POP   PSW      UNLOAD STACK
0098 F1                1480          POP   PSW      GET MASTER PATTERN
0099 17                1485          RAL            SHIFT STARTING PATTERN
009A DA A6 00          1490          JC    TST2     TEST 1 IS COMPLETE. DO TEST 2
009D E1                1495          POP   H        GET START
009E 22 5A 01          1500          SHLD  BBUF     STORE START
00A1 E5                1505          PUSH  H        SAVE START
00A2 F5                1510          PUSH  PSW      SAVE MASTER PATTERN
```

```
00A3 C3 6F 00          1515          JMP    WRL1    CONTINUE TEST 1
00A6                   1520 *
00A6 E1                1525 TST2     POP    H       RESTORE START ADDR
00A7 22 5A 01          1530          SHLD   BBUF    STORE START ADDRESS
00AA E5                1535          PUSH   H       SAVE START ADDRESS
00AB AF                1540          XRA    A       INITIALIZE MASTER PATTERN
00AC 37                1545          STC            SET CARRY
00AD F5                1550          PUSH   PSW     SAVE MASTER PATTERN
00AE                   1555 *
00AE F5                1560 WRL2     PUSH   PSW     SAVE WORKING PATTERN
00AF 77                1565          MOV    M,A     WRITE PATTERN TO MEMORY
00B0 CD 4B 00          1570          CALL   ACHK    INCR LOCATION, AND CHECK
00B3 DA BB 00          1575          JC     RDL3    DONE WRITING
00B6 F1                1580          POP    PSW     RESTORE PATTERN
00B7 1F                1585          RAR            SHIFT PATTERN
00B8 C3 AE 00          1590          JMP    WRL2    DO MORE
00BB                   1595 *
00BB F1                1600 RDL3     POP    PSW     UNLOAD STACK
00BC F1                1605          POP    PSW     GET MASTER PATTERN
00BD E1                1610          POP    H       GET START
00BE 22 5A 01          1615          SHLD   BBUF    STORE START
00C1 E5                1620          PUSH   H       SAVE START
00C2 F5                1625          PUSH   PSW     SAVE MASTER PATTERN
00C3                   1630 *
00C3 F5                1635 RDL4     PUSH   PSW     SAVE PATTERN
00C4 BE                1640          CMP    M       CHECK IT
00C5 C4 F4 00          1645          CNZ    MTER    ERROR
00C8 CD E5 00          1650          CALL   ESCP    CHECK FOR ESCAPE
00CB CD 4B 00          1655          CALL   ACHK    INCR LOCATION CHECK IF LAST
00CE DA D6 00          1660          JC     NXP2    NEXT PATTERN
00D1 F1                1665          POP    PSW     GET WORKING PATTERN
00D2 1F                1670          RAR            SHIFT WORKING PATTERN
00D3 C3 C3 00          1675          JMP    RDL4    DO MORE READING
00D6                   1680 *
00D6 F1                1685 NXP2     POP    PSW     UNLOAD STACK
00D7 F1                1690          POP    PSW     GET MASTER PATTERN
00D8 1F                1695          RAR            SHIFT PATTERN
00D9 DA 0A 01          1700          JC     MTCP    MEMORY TEST COMPLETE MESSAGE
00DC E1                1705          POP    H       RESTORE START
00DD 22 5A 01          1710          SHLD   BBUF    STORE START
00E0 E5                1715          PUSH   H       SAVE START
00E1 F5                1720          PUSH   PSW     SAVE MASTER PATTERN
00E2 C3 AE 00          1725          JMP    WRL2    DO MORE
00E5                   1730 *
00E5 DB 00             1735 ESCP     IN     VIDS    ANYBODY KNOCK?
00E7 E6 40             1740          ANI    40H     STATUS MASK
00E9 C8                1745          RZ             NO, CONTINUE
00EA DB 01             1750          IN     KBDI    YES, WHAT WAS IT?
00EC E6 7F             1755          ANI    7FH     PARITY MASK
00EE FE 1B             1760          CPI    1BH     ESC ?
00F0 CA 03 00          1765          JZ     BGIN    RESTART
00F3 C9                1770          RET            NOT AN ESCAPE, CONTINUE
00F4                   1775 *
00F4                   1780 * THIS ROUTINE MAPS ERRORS
00F4                   1785 * INTO EBUF AREA
00F4                   1790 *
00F4 D1                1795 MTER     POP    D
00F5 F1                1800          POP    PSW     /GET WRITE PATTERN
```

```
00F6 F5             1805          PUSH  PSW
00F7 D5             1810          PUSH  D
00F8 AE             1815          XRA   M       /EXOR READ PATTERN
00F9 47             1820          MOV   B,A     /SAVE IN B
00FA 3A 5B 01       1825          LDA   BBUF+1
00FD E6 0C          1830          ANI   0CH
00FF 0F             1835          RRC
0100 0F             1840          RRC
0101 21 52 01       1845          LXI   H,EBUF
0104 85             1850          ADD   L       /COMPUTE MAP POINTER
0105 6F             1855          MOV   L,A
0106 7E             1860          MOV   A,M
0107 B0             1865          ORA   B       /PUT ERRORS IN MAP
0108 77             1870          MOV   M,A
0109 C9             1875          RET
010A                1880 *
010A                1885 *  GET HERE WHEN PASS COMPLETE
010A                1890 *
010A 3A 6E 01       1895 MTCP     LDA   DBUF+4
010D 3C             1900          INR   A
010E 32 6E 01       1905          STA   DBUF+4
0111 FE 04          1910          CPI   4
0113 CA 1D 01       1915          JZ    PRINT /AFTER 4 PASSES
0116 E1             1920          POP   H
0117 22 5A 01       1925          SHLD  BBUF
011A C3 68 00       1930          JMP   MRC1
011D                1935 *
011D                1940 * THIS ROUTINE PRINTS THE MAP
011D                1945 *
011D 0E 04          1950 PRINT    MVI   C,4
011F 21 55 01       1955          LXI   H,EBUF+3
0122 5E             1960 LOOP1    MOV   E,M
0123 16 08          1965          MVI   D,8
0125 CD 38 00       1970          CALL  CRLF
0128 7B             1975 LOOP2    MOV   A,E
0129 07             1980          RLC
012A 5F             1985          MOV   E,A
012B 06 47          1990          MVI   B,'G'
012D D2 32 01       1995          JNC   PAST
0130 06 58          2000          MVI   B,'X'
0132 CD 2D 00       2005 PAST     CALL  OUT8
0135 15             2010          DCR   D
0136 C2 28 01       2015          JNZ   LOOP2
0139 2B             2020          DCX   H
013A 0D             2025          DCR   C
013B C2 22 01       2030          JNZ   LOOP1
013E CD 38 00       2035          CALL  CRLF    / DONE
0141 CD 38 00       2040          CALL  CRLF
0144 CD E5 00       2045 LOOP3    CALL  ESCP
0147 C3 44 01       2050          JMP   LOOP3
014A                2055 *
014A 00             2060 FIN      NOP   END OF PROGRAM - REF LAST LOCATION
014B                2065 *
014B                2070 SCRA     EQU   FIN     AFTER THIS AREA
014B                2075 EBUF     EQU   SCRA+8H   (08) ERROR MAP AREA
014B                2080 BBUF     EQU   SCRA+10H  (16) BINARY BUFFER
014B                2085 DBUF     EQU   SCRA+20H  (16) DATA BUFFER
014B                2090 AREA     EQU   SCRA+40H  (32) STACK AREA
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014B                    2095 VIDS   EQU   0       STATUS PORT
014B                    2100 VIDO   EQU   1       DATA OUT PORT
014B                    2105 KBDI   EQU   1       KEYBOARD INPUT PORT
014B                    2110 SP     EQU   6       STACK POINTER
014B                    2115 PSW    EQU   6       ACC & FLAGS
SYMBOL  VALUE     LINE NUMBER REFRENCE
ACH1    005D      1260 1275
ACHK    004B      1360 1445 1570 1655
AREA    018A      1065
BBUF    015A      1100 1125 1150 1245 1250 1265 1295 1320 1405 1500 1530
                  1615 1710 1825 1925
BGIN    0003      1765
CRLF    0038      1070 1970 2035 2040
DBUF    016A      1315 1895 1905
EBUF    0152      1110 1115 1845 1955
ESCP    00E5      1440 1650 2045
FIN     014A
INSS    0009      1085
KBDI    0001      1060 1750
LOOP1   0122      2030
LOOP2   0128      2015
LOOP3   0144      2050
MRC1    0068      1930
MRCK    0062      1155
MTCP    010A      1700
MTER    00F4      1435 1645
NXP1    0097      1450
NXP2    00D6      1660
OUT8    002D      1175 1205 1215 1225 1230 2005
PAST    0132      1995
PRINT   011D      1915
PSW     0006      1340 1350 1370 1390 1395 1415 1425 1455 1475 1480 1510
                  1550 1560 1580 1600 1605 1625 1635 1665 1685 1690 1720 1800
                  1805
RDL1    007C      1365
RDL2    0084      1465
RDL3    00BB      1575
RDL4    00C3      1675
SCRA    014A
SP      0006      1065
TST2    00A6      1490
VIDO    0001      1185
VIDS    0000      1165 1735
WRL1    006F      1380 1515
WRL2    00AE      1590 1725
```