

DESIGNING CONSUMER- SYSTEM PERIPHERALS

INTELLIGENT-TERMINAL DESIGNERS OPT FOR 8080-COMPATIBLE CIRCUITRY

by Lee Felsenstein and Robert Marsh

Because the "home computer" serves a consumer market, both it and the peripherals designed for use with it must exhibit high-volume production and adequate customer support. With these fundamental requirements in mind, we designed the Sol product line to simultaneously meet the needs of two applications. Both Sol-10 and Sol-20 function as intelligent terminals—each unit lacks only a CRT monitor. Additionally, Sol-20 incorporates a power supply and expansion chassis, which with adequate memory allow it to operate as a stand-alone computer. And the system's basic electronics, housed on one board and designated Sol-PC, serves OEM applications that require a single-board computer.

To provide Sol with the required customer support, we developed Basic and Focal language packages as well as application and game programs. We also developed two ROM-resident programs—Solos, which optimizes Sol-20 functions for stand-alone computer applications, and Soled, which implements the functions of an intelligent terminal on either Sol-10 or Sol-20.

Lee Felsenstein is the founder of LGC Engineering, Berkeley, CA, and a consultant to Processor Technology, Emeryville, CA. Robert Marsh is vice president of Processor Technology.

All of these actions hinged on one major development in the hobby-computer market. Within the past year, several peripheral-interface and memory kits have appeared, each of which utilizes the "hobbyist," or S-100, bus structure used in several 8080-based computers. To take advantage of such kits, we decided to design the Sol family around this same S-100 bus structure. In essence, Sol is the combination of a microprocessor circuit with several S-100 peripheral modules.

implementing the design

As initially conceived by one of us (Marsh), Sol consists of a typewriter-sized cabinet on whose flat top a video monitor

can rest (Fig 1). One 10" x 16" PC card contains all electronics except the unit's keyboard and power supply, and the video signal generated by the device serves any EIA-standard monitor. A PC edge connector on the board accepts a backplane daughter board that holds as many as five S-100 cards. All I/O connectors, also available on the rear edge of the PC card, are accessible from the cabinet's rear.

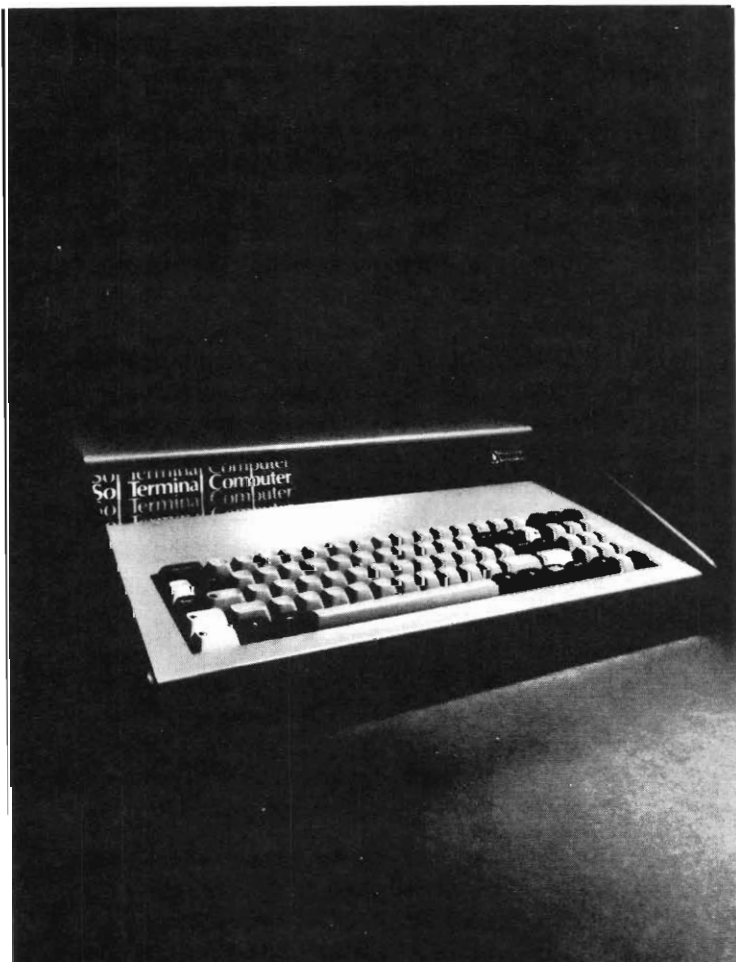
To implement this basic structure (Fig 2), we buffered the system's 8080 address and data lines to the circuit and bus connector through tri-state drivers, much as do other S-100-type processors. Next, we paralleled two unidirectional data buses to form a bidirectional bus and thereby eliminated the need to run eight additional lines around what promised and proved to be a very crowded card. We also connected a 4-input multiplexer to select data input to the processor from the keyboard port, the parallel port and an internal data bus, as well as from the external data bus.

We created the internal bus as a unidirectional circuit for low-drive, on-card memory and I/O devices that cannot meet the heavy drive requirement of the full external data bus; it allows maximum utilization of the tri-state capabilities of the universal asynchronous receiver/transmitters (UARTs) used in the serial and tape channels. The flag and status outputs of these devices arrive in parallel at the 8080 chip; port addresses from the board's address decoder section enable the outputs. The decoder also controls the multiplexer's switching; default direction comes from the system's external bus. We defined the 4K bytes of memory in Page C (high-order hex digit of the address) as on-card memory, divided between 2K of ROM, 1K of RAM and 1K of "visible RAM" in the video display circuit.

The display section treats its RAM as 2-port memory; the processor has the highest priority. We placed the second port under control of the screen refresh circuitry, which calls up data as required for conversion by the character-generator ROM into video signals for display. We didn't connect the video display section to the internal bus because we felt we had to allow for its being loaded directly from an external DMA device, which can gain control of the data bus but not the internal bus. We made the data bus the source of all data fed to memory and I/O, both on-card and off; the only other data input to the processor from on-card circuitry through the data bus comes from the sense switches, an 8-wide DIP array that lets the CPU sense an alterable parameter byte under program control through input port FF.

We derived board timing from a 14.31818-MHz crystal oscillator; the frequency, four times that of the NTSC color burst, provides compatibility with color video graphics devices. This "dot clock" goes to an external connector and feeds the output shift register and character divider of the video display section as well as the 8080 clock divider. We configured the clock circuit using MSI and SSI TTL chips rather than the Intel 8224 LSI chip to allow for several selectable microprocessor clock rates; that way, we can retrofit higher-speed processor chips into the same board. When designing the clock, we took care to ensure non-overlapping

Fig 1 Housed in a typewriter-sized cabinet on which a CRT monitor can sit, Sol-20 contains all circuitry necessary to function either as an intelligent terminal or a stand-alone computer. The system's designers chose to configure it around the "hobbyist," or S-100, bus structure used in several 8080-based computers; Sol is basically the combination of several S-100 peripheral modules with a microprocessor circuit.



phases and used a switch-tail ring counter to eliminate ambiguous states during clocking. An AH 0026 dual MOS clock-driver chip feeds the 8080.

The circuitry synchronizes all control inputs to the 8080 with the clock and forces a "wait state" immediately after the reset condition; these two techniques help eliminate

the use of higher-speed 8080 chips without requiring replacement of on-card memory. High-speed access still occurs to all off-card memory that resides on the bus.

The serial interface drives its baud clock from a 1200-Hz signal extracted from a divider in the video display section. A 153.6-kHz signal locks to this lower frequency through a

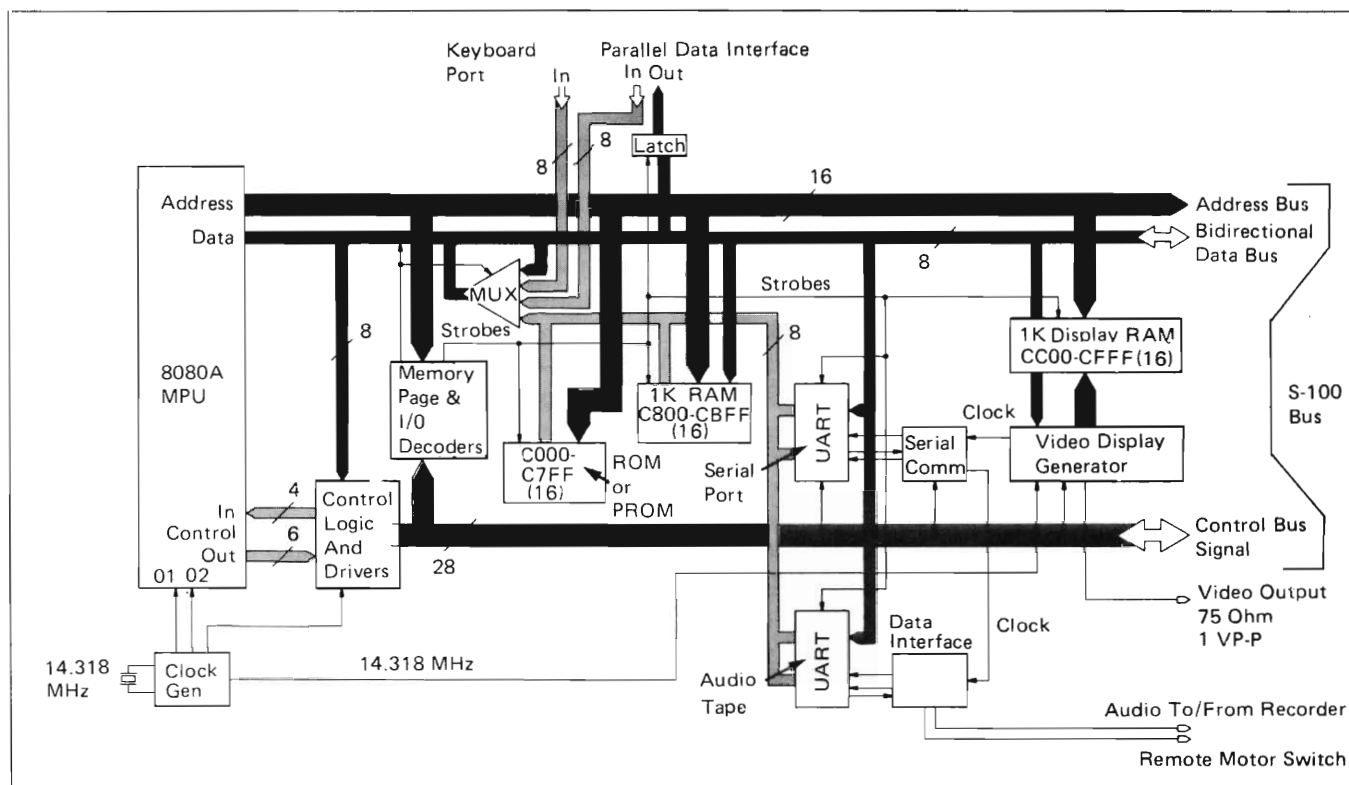


Fig 2 The internal bus in the Sol circuitry functions as a unidirectional circuit for low-drive, on-card memory and I/O devices that can't meet the drive requirement of the system's full external data bus.

It allows Sol to fully utilize the tri-state capabilities of the UARTs used in the intelligent-terminal system's serial-interface and tape-interface channels.

"crash" conditions to which previous S-100 processors are prone. An R-C charge-up network provides automatic power-up reset sequencing of the processor.

The 8080 initializes with its program counter at 0000, but much software currently in use, as well as the vectored interrupt instruction subset in the 8080, requires the location of RAM at Page 0. To allow for temporary relocation of ROM to Page 0 during the first four fetches after reset, we configured a "phantom" circuit, which provides a signal to a bus pin during that period; the memory-page decoder consists of exclusive ORs that respond to C or 0 depending on the state of this circuit. The first instruction in the ROM is always a NOP, followed by a Jump to the first page of C000, so when the "phantom" signal ceases the program counter is set to the location in ROM where it will next appear.

We placed the ROM on a 1.75" x 3.5" plug-in personality module card that fits into a 30-pin edge connector at the rear of the unit. Originally implemented to allow for multiple EPROM sourcing, this connection method also lets unskilled users interchange monitor firmware without removing the cabinet.

interfaces

Sol's parallel interface circuit follows the model of the hobbyist standard proposed by Harold Mauch of Percom, Inc. Because this standard calls for a minimum strobe width of 1 μ s for interfacing to MOS logic, we inserted a wait state in all I/O operations to widen their strobes. The video display also requires a wait state to allow for settling of the 2-port address multiplexers, so we decided to insert one wait state in all on-card memory references. The insertion allows

CMOS 4046 phase-locked loop that works through a 4024 CMOS divider; the divider's outputs provide clocks for all rates between 75 and 9600 baud, except 110 baud. For that rate, a 4029 CMOS programmable counter performs a divide-by-eleven on a 19.2-kHz signal and produces a 109-baud clock. The outputs of the divider also function as timing signals in the tape interface section.

The tape interface allows data recording at 1200 baud on audio cassettes or other audio media; it uses Manchester or phase encoding with a bit-cell time of 1667 μ s. In response to suggestions originally made by Don Lancaster of Synergetics, the interface feeds a UART with a clock that is phase-locked to the incoming data rate and thereby assures recovery of the data independent of real-time distortion introduced by tape-speed variation over the lock range of the loop. Automatic gain control provides another necessary dimension of adaptability. This recording and recovery method, termed CUTS (Computer Users Tape Standard), represents a refinement of the "Kansas City" or "Byte" standard defined in 1975. The audio tape interface is software-switchable between these two standards, and two motor-control relays on the Sol board replace the switches of the usual low-cost cassette recorder.

The system's keyboard, a custom unit from Key Tronic, connects to the PC board through a ribbon cable connector that plugs into a header soldered to the board. A capacitance crossbar-type unit that uses no LSI encoder and no mechanical contacts, the unit has a key assembly that can be removed for cleaning in case of the dreaded "Coke Test." A combination of "upper case" and "repeat" keys performs a reset function and eliminates the need for a reset switch.